IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PROMOS TECHNOLOGIES, INC., Plaintiff, v. FREESCALE SEMICONDUCTOR, INC., Defendant.	)	C.A. No. 06-788 (JJF)

APPENDIX TO FREESCALE'S OPENING CLAIM CONSTRUCTION BRIEF
VOLUME I: EXHIBITS RELATING TO THE FORTIN PATENT

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EXHIBIT A

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(12) **United States Patent**
Fortin

(10) **Patent No.: US 6,670,267 B2**
(45) **Date of Patent: Dec. 30, 2003**

(54) **FORMATION OF TUNGSTEIN-BASED INTERCONNECT USING THIN PHYSICALLY VAPOR DEPOSITED TITANIUM NITRIDE LAYER**

(75) Inventor: **Vincent Fortin**, Santa Clara, CA (US)

(73) Assignee: **Mosel Vitelic Inc.**, Hsin Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**[7] **H01L 21/4763**; H01L 29/12

(52) **U.S. Cl.** **438/629**; 438/637; 438/667; 438/700; 257/915

(58) **Field of Search** 257/758, 752, 257/753, 774, 775, 915; 438/118, 222, 622, 690–693, 687, 758, 316, 632–634, 720, 784, 629, 637, 643, 644, 667, 750, 700

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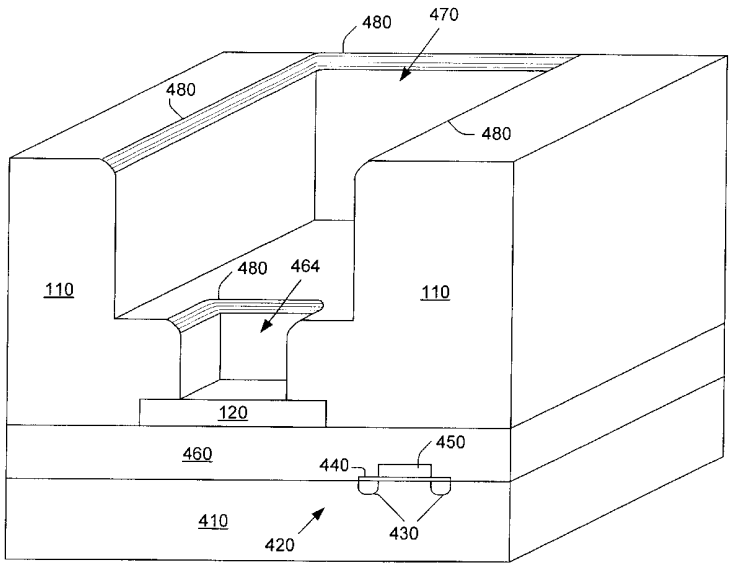
(57) **ABSTRACT**

A tungsten-based interconnect is created by first providing a structure with an opening **(464/470)** in a structure and then rounding the top edge of the opening. A titanium nitride layer **(150)** is physically vapor deposited to a thickness less than 30 nm, typically less than 25 nm, over the structure and into the opening. Prior to depositing the titanium nitride layer, a titanium layer **(140)** may be deposited over the structure and into the opening such that the later-formed titanium nitride layer contacts the titanium layer. In either case, the titanium nitride layer is heated, typically to at least 600° C., while being exposed to nitrogen and/or a nitrogen compound. A tungsten layer **(160)** is subsequently chemically vapor deposited on the titanium nitride layer and into the opening.

54 Claims, 4 Drawing Sheets



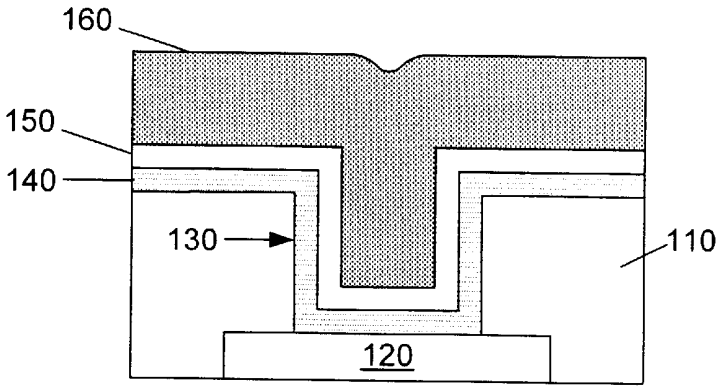


FIG. 1 PRIOR ART

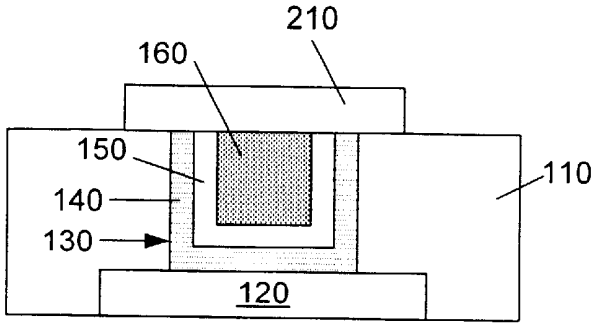


FIG. 2 PRIOR ART

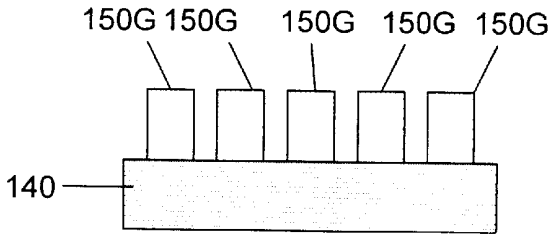


FIG. 3 PRIOR ART

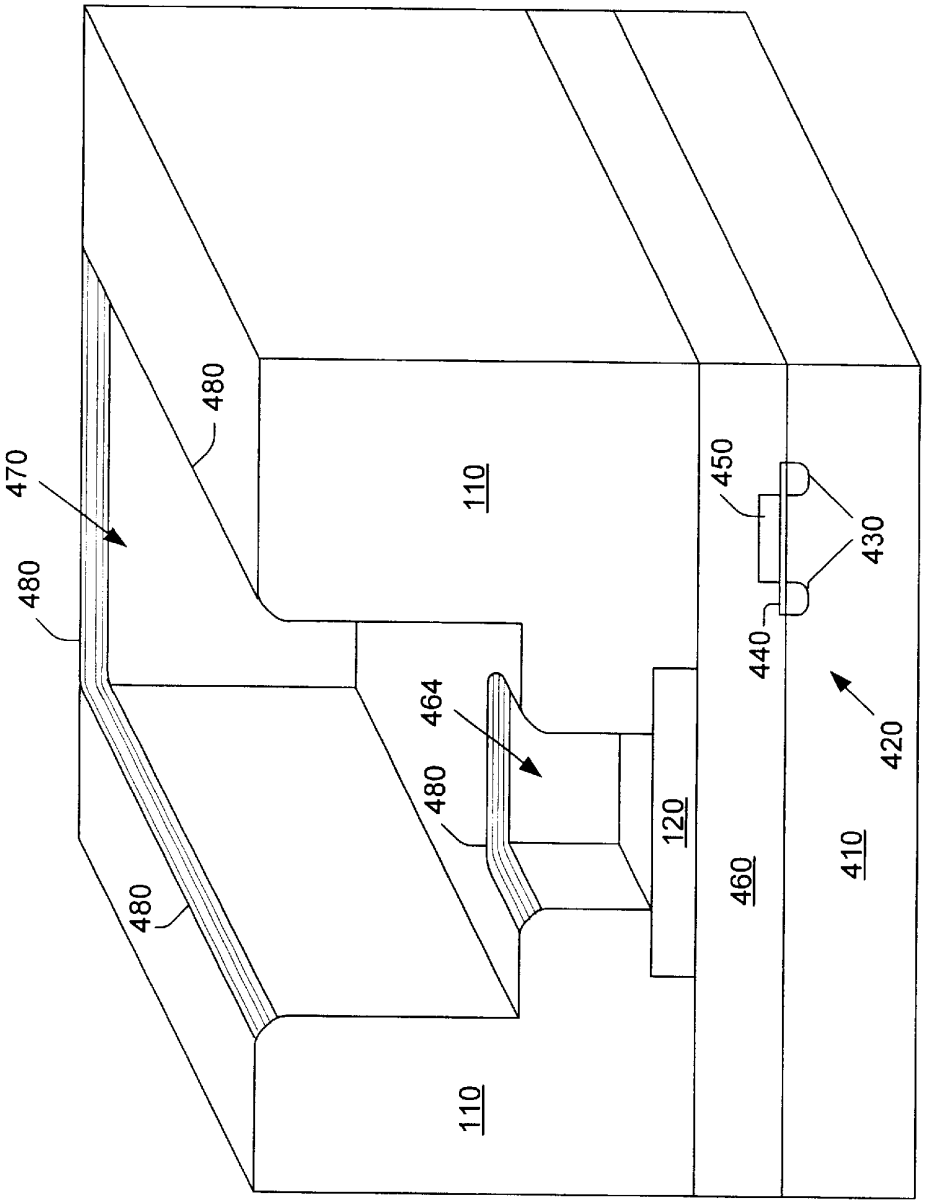


FIG. 4

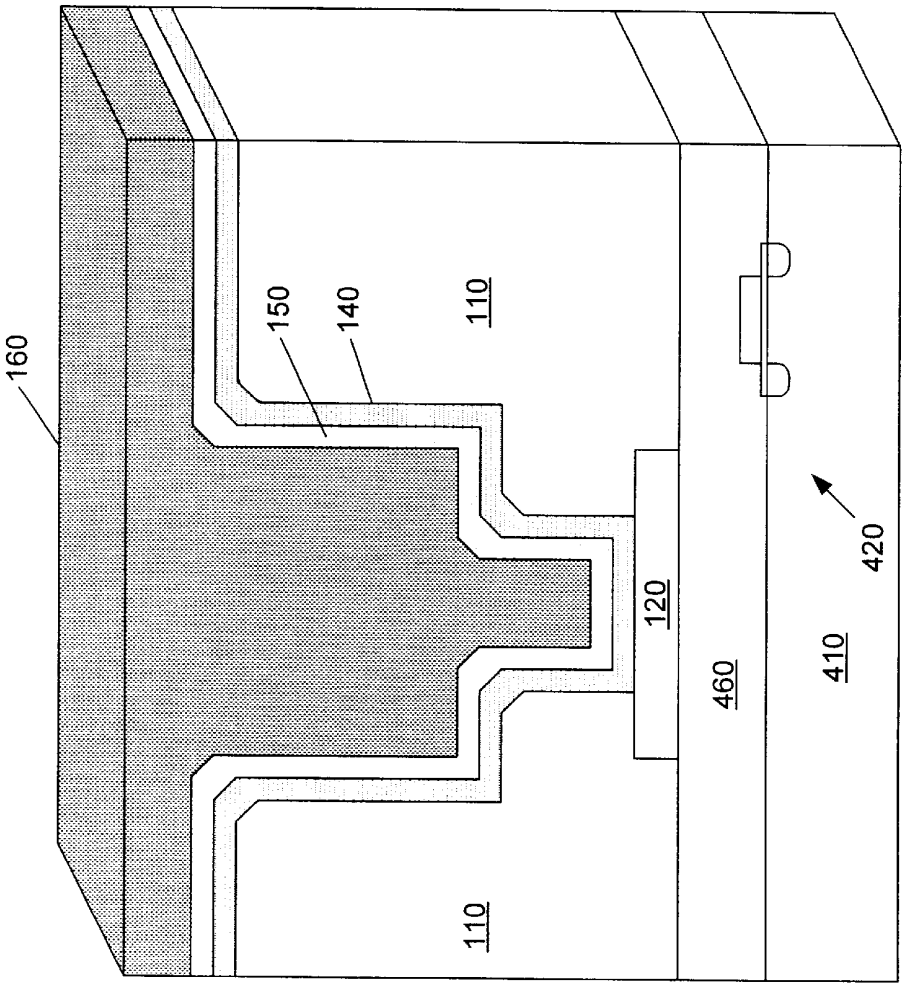


FIG. 5

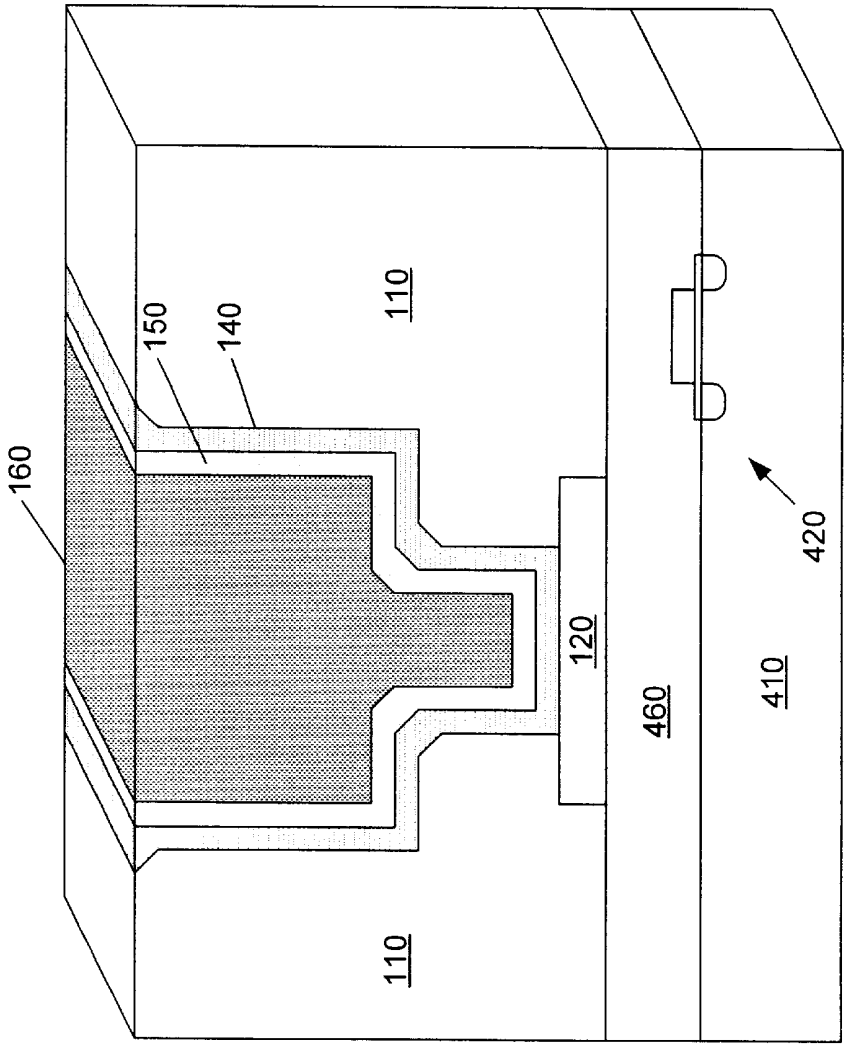


FIG. 6

FORMATION OF TUNGSTEIN-BASED INTERCONNECT USING THIN PHYSICALLY VAPOR DEPOSITED TITANIUM NITRIDE LAYER

BACKGROUND

The present invention relates to physical vapor deposition of titanium nitride.

Titanium nitride has been used as a barrier and adhesion layer in fabrication of tungsten plugs in semiconductor integrated circuits. Tungsten plugs interconnect different conductive layers separated by a dielectric. Frequently used dielectrics are silicon dioxide and silicon nitride. Tungsten does not adhere well to silicon dioxide and silicon nitride, so titanium nitride has been used to promote adhesion. In addition, titanium nitride serves as a barrier layer preventing a chemical reaction between WF_6 (a compound from which the tungsten is deposited in a chemical vapor deposition process) and other materials present during tungsten deposition. See "Handbook of Semiconductor Manufacturing Technology" (2000), edited by Y. Nichi et al., pages 344–345.

FIGS. **1**, **2** illustrate a typical fabrication process. A dielectric layer **110** is deposited over a layer **120** which can be a metal or silicon layer. A via **130** is etched in the dielectric. A thin titanium layer **140** is deposited over dielectric **110** and into the via **130** to improve contact resistance (the titanium dissolves the native oxide on layer **120**). Then titanium nitride layer **150** is deposited. Then tungsten **160** is deposited by chemical vapor deposition (CVD) from tungsten hexafluoride (WF_6). Tungsten **160** fills the via. Layers **160**, **150**, **140** are removed from the top surface of dielectric **110** (by chemical mechanical polishing or some other process). See FIG. **2**. The via remains filled, so the top surface of the structure is planar. Then a metal layer **210** is deposited. The layers **160**, **150**, **140** in via **130** provide an electrical contact between the layers **210** and **120**.

Titanium nitride **150** can be deposited by a number of techniques, including sputtering and chemical vapor deposition (CVD). Sputtering is less complex and costly (see "Handbook of Semiconductor Manufacturing Technology", cited above, page 411), but the titanium nitride layers deposited by sputtering have a more pronounced columnar grain structure. FIG. **3** illustrates columnar monocrystalline grains 150 G in titanium nitride layer **150**. During deposition of tungsten **160**, the WF_6 molecules can diffuse between the TiN grains and react with titanium **140**. This reaction produces titanium fluoride TiF_3. TiF_3 expands and causes failure of the TiN layer. The cracked TiN leads to a higher exposure of TiF_3 to WF_6, which in turn leads to the formation of volatile TiF_4. TiF_4 causes voids in the W film which are known as "volcanoes". To avoid the volcanoes, the sputtered titanium nitride layers have been made as thick as 40 nm, and at any rate no thinner than 30 nm. In addition, the sputtered titanium nitride layers have been annealed in nitrogen atmosphere to increase the size of the TiN grains.

SUMMARY

The inventor has determined that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers. In some embodiments, fewer volcanoes have been observed with a TiN layer thickness of 20 nm than with 30 nm. In fact, no volcanoes have been observed in some structures formed with the 20 nm TiN layers. Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers and a higher density of the TiN grains.

The invention is applicable to physical vapor deposition techniques other than sputtering. Additional features and embodiments of the invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1–3** are cross sectional views of prior art semiconductor structures in the process of fabrication.

FIGS. **4–6** are cross sectional and perspective views of semiconductor structures in the process of fabrication according to one embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. **4** is a cross sectional and perspective view of a dual damascene semiconductor structure in the process of fabrication according to one embodiment of the present invention. Layer **120** is polysilicon formed by chemical vapor deposition (CVD) over a monocrystalline silicon wafer **410**. Before fabrication of layer **120**, the wafer **410** may have been processed to form devices such as MOS transistor **420**. The transistor's source/drain regions **430** were formed in substrate **410**, gate insulation **440** was formed over the substrate, and gate **450** was formed over the gate insulation. Other devices, including non-MOS devices, could be formed using known techniques. Layer **120** can also be part of substrate **410** (this embodiment is not shown in FIG. **4**).

In the embodiment of FIG. **4**, dielectric **460** was deposited over the wafer. Then layer **120** was formed as described above, and was patterned by a plasma etch. An exemplary thickness of layer **120** is 150 nm.

Dielectric layer **110** was deposited over the layer **120**. In some embodiments, dielectric **110** was a combination of two silicon dioxide layers. The first layer was PSG (phosphosilicate glass) deposited by chemical vapor deposition (CVD). The second layer was silicon dioxide deposited by CVD from TEOS. The combined thickness of the two layers was approximately 900 nm.

Then a photoresist layer (not shown) was deposited and patterned photolithographically to define a via **464**. In some embodiments, the mask opening defining the via was round in top view, with a diameter of 0.18 μm. The via was formed in layer **110** with a plasma etch.

The photoresist was removed, and another layer of photoresist (not shown) was deposited and patterned photolithographically to define a trench **470** in dielectric **110** for a tungsten interconnect. The length of the trench **470** was normally at least 2 μm. In some embodiments, the trench length was approximately 1 mm. The trench width was then 0.22 μm. The trench was etched with a timed etch to a depth of approximately 250 nm. Via **464** was fully exposed at the bottom of the trench.

Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. The argon flow was 5 sccm (standard cubic centimeters per minute). The RF power was 315 W. This operation removed native oxide from layer **120**. Also, this operation smoothened (rounded) top edges **480** of trench **470** and via **464**, i.e., the respective perimetrical top edges formed by the perimeters of trench **470** and via **464** along the surfaces into which they respectively extend. The rounded perimetrical top edges are desir-

able to reduce stress in titanium nitride **150** (FIG. **5**) at these edges so as to reduce the risk of volcano formation. The RF plasma operation was performed in a system of type ENDURA available from Applied Materials of Santa Clara, Calif.

Then titanium layer **140** (FIG. **5**) was sputter deposited from a titanium target. The sputtering was performed at a temperature of 200° C. in argon atmosphere. The base pressure (the pressure before the argon flow was turned on) was 5×10^{-7} torr. The DC power was 4000 W, the RF power was 2500 W. The wafer AC bias was 150 W. The titanium deposition was performed in a system of type ENDURA, in an ionized metal plasma (IMP) chamber of type Vectra, available from Applied Materials.

The thickness of Ti layer **140** was varied. In one embodiment, the thickness was less than 36 nm, preferably less than 15 nm, more preferably less than 12 nm, typically 10 nm. In another embodiment, the thickness was 36 nm.

Then titanium nitride **150** was deposited by reactive sputtering from a titanium target in a nitrogen atmosphere. The base pressure (the pressure before the nitrogen flow was turned on) was 5×10^{-7} torr. The nitrogen flow was 28 sccm (standard cubic centimeters per minute), the DC power was 4000 W, the RF power was 2500 W, the wafer bias was 150 W. The deposition temperature was 200° C. The deposition was performed in a system of type ENDURA, in an IMP chamber of type Vectra, available from Applied Materials.

In one embodiment, the thickness of TiN layer **150** was less than 30 nm, preferably less than 25 nm, more preferably less than 22 nm, typically 20 nm. The thickness of the TiN layer **150** was 30 nm in another embodiment.

Then the structure was heated to a temperature between 600° C. and 700° C. for 20 to 40 seconds, typically 20 to 30 seconds, in a nitrogen atmosphere. (This operation is referred to herein as Rapid Thermal Anneal, or RTA.) The base pressure was 100–120 torr, the nitrogen flow was **8** slm (standard liters per minute). The temperature was 620° C. in one embodiment, 670° C. in another embodiment. The anneal was performed in a system of type HEATPULSE 8800 available from AG Associates, Inc., of San Jose, Calif. The anneal is believed to have increased the lateral size of TiN grains 150G (FIG. **3**).

Then tungsten layer **160** was deposited by CVD in two stages. At the first stage, the chemical reaction was:

$$2WF_6+3SiH_4\rightarrow 2W+3SiF_4+6H_2$$

This stage lasted 10 seconds. Then the silane (SiH_4) flow was turned off, and the hydrogen flow was turned on for the second stage. The chemical reaction was:

$$WF_6(\text{vapor})+3H_2\ (\text{vapor})\rightarrow W(\text{solid})+6HF(\text{vapor}).$$

See S. Wolf, "Silicon Processing for the VLSI Era", vol. 2 (1990), page 246, incorporated herein by reference. Both stages were performed in a system of type CONCEPT 1 available from Novellus Systems of San Jose, Calif. The silane flow was 20 sccm. The hydrogen flow was 12–15 slm (standard liters per minute). The WF_6 flow was 350 sccm. The pressure was 40 torr. The temperature was 400° C.

Then the layers **160**, **150**, **140** were polished off the top of dielectric **110** by CMP. The resulting structure is shown in FIG. **6**. Prior to CMP, the structure was examined for volcanoes using an optical microscope and SEM and STEM microscopes. The results are given in Table 1 below. The second column of Table 1 indicates the temperature of the Rapid Thermal Anneal, described above, performed after the deposition of TiN **150** before the deposition of tungsten **160**. In Embodiment No. 1, the anneal was omitted.

TABLE 1

Embodiment No.	RTA of TiN	Ti/TiN thickness: 10 nm/20 nm Volcanoes observed?	Ti/TiN thickness: 36 nm/30 nm Volcanoes observed?
1.	None	Yes	Yes
2.	620° C.	No	Yes, but fewer than in Embodiment No. 1
3.	670° C.	No	No

These results show, unexpectedly, that the use of thinner Ti and TiN layers in combination with the RTA can provide a better protection against the volcanoes than thicker layers without the RTA. The thinner layers can eliminate the volcanoes at the lower RTA temperature of 620° C. Lower RTA temperatures are desirable to reduce impurity diffusion during the RTA, to prevent melting or softening of materials having low melting temperatures (e.g. aluminum), and reduce wafer warping. In any event, the sputter deposited TiN layers, such as TiN layer **150**, have substantially a columnar grain structure.

The invention is not limited to the particular materials, dimensions, structures, or fabrication processes described above. The invention is not limited to a thickness or composition of any particular layer, or the number, shape and size of vias **464** or trenches **470**. The trench length, for example, is 2 μm in some embodiments, and other lengths are possible. The invention is not limited to the particular gas flow rates, temperatures, or any other fabrication parameters or equipment. Some embodiments use nitrogen sources other than pure nitrogen for the RTA or titanium nitride deposition. For example, ammonia (NH_3) or H_2/N_2 can be used. The invention is not limited to the Rapid Thermal Anneal or to any particular anneal temperature. Non-rapid anneals can be used. The anneal can be performed with plasma or with other heating techniques, known or to be invented. The invention is applicable to TiN sputtered from a TiN target. The invention is applicable to single damascene, dual damascene, and other structures, for example, to tungsten plugs formed in contact vias in non-damascene structures, and to tungsten features other than plugs. Titanium **140** is omitted in some embodiments. The invention is applicable to different tungsten CVD techniques, including tungsten deposition from WCl_6 rather than WF_6. The invention is not limited by particular materials chosen for the layers **120**, **110**, **460**. Some embodiments involve non-silicon semiconductor materials. The invention is not limited to any particular sputtering process, and further is applicable to TiN deposited by physical vapor deposition techniques other than sputtering. For example, pulsed laser deposition and other evaporation techniques can be used. See "Handbook of Semiconductor Manufacturing Technology" (2000), cited above, pages 395–413, incorporated herein by reference. Layer **120** (FIG. **4**) can be a metal layer, and can be part of the second, third, or higher metallization layers. The term "layer", as used herein, may refer to a combination of two or more other layers. The invention is defined by the appended claims.

I claim:

1. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 25 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

2. The method of claim **1** wherein the titanium nitride layer is formed by sputtering.

3. The method of claim **2** wherein the titanium nitride layer is less than 22 nm thick.

4. The method of claim **2** wherein the titanium nitride layer is about 20 nm thick.

5. The method of claim **1** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

6. The method of claim **5** wherein the titanium layer is less than 36 nm thick.

7. The method of claim **5** wherein the titanium layer is about 10 nm thick.

8. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600° C.

9. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 670° C. for 20–40 seconds.

10. The method of claim **1** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 620° C. for 20–40 seconds.

11. The method of claim **1** wherein:

the structure comprises (a) a substrate, (b) a circuit element situated in or over the substrate, and (c) an insulating layer situated over the circuit element and the substrate, the opening in the structure comprising an opening in the insulating layer, the opening in the insulating layer comprising a trench at least 2 μm long;

the titanium nitride layer and the tungsten layer extend into the opening in the insulating layer; and

the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening in the insulating layer.

12. The method of claim **11** wherein the substrate is a semiconductor substrate.

13. The method of claim **12** wherein the trench is at least 1 mm long.

14. The method of claim **13** further comprising, before forming the titanium nitride layer, depositing a titanium layer over the insulating layer such that the titanium layer extends at least into an opening in the insulating layer and such that the tungsten layer electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening in the insulating layer.

15. The method of claim **14** wherein the trench does not penetrate the insulating layer but a via at the bottom of the trench penetrates the insulating layer and exposes the circuit element, wherein the titanium layer physically contacts the circuit element at the bottom of the via.

16. The method of claim **13** wherein the circuit element is conductive.

17. The method of claim **13** wherein the circuit element comprises metal or semiconductor material.

18. The method of claim **13** wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.

19. A structure formed by the method of claim **1**.

20. The structure of claim **19** wherein the titanium nitride layer has a substantially columnar grain structure.

21. A structure formed by the method of claim **2**.

22. The structure of claim **21** wherein the titanium nitride layer has a substantially columnar grain structure.

23. The method of claim **1** where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

24. The method of claim **23** wherein the tungsten halide comprises tungsten hexafluoride.

25. A method for fabricating an integrated circuit, the method comprising:

forming a circuit element in or over a semiconductor substrate;

forming an insulating layer over the circuit element;

forming an opening through the insulating layer to expose the circuit element at the bottom of the opening, the opening having a perimetrical top edge that extends along an exterior surface of the insulating layer;

rounding the top edge of the opening;

forming a titanium layer over the insulating layer, the titanium layer overlaying side and bottom surfaces of the opening, the titanium layer being less than 15 nm thick;

forming a titanium nitride layer over the titanium layer, the titanium nitride layer being less than 25 nm thick, the titanium nitride layer being formed by sputtering;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and

forming a tungsten layer by chemical vapor deposition over the titanium nitride layer, the tungsten layer at least partially filling the opening and electrically contacting the circuit element through the titanium and titanium nitride layers.

26. The method of claim **25** wherein the opening comprises a trench at least 2 μm long.

27. The method of claim **25** wherein the opening comprises a trench at least 1 mm long.

28. The method of claim **25** wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 670° C. for 20–40 seconds.

29. The method of claim **25** wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 620° C. for 20–40 seconds.

30. The method of claim **25** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600° C.

31. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride

layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer to a temperature above 600° C. while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

32. The method of claim **31** wherein the titanium nitride layer is formed by sputtering.

33. The method of claim **31** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

34. The method of claim **33** wherein the titanium layer is less than 36 nm thick.

35. The method of claim **31** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 670° C. for 20–40 seconds.

36. The method of claim **31** wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 620° C. for 20–40 seconds.

37. The method of claim **31** wherein:

the structure comprises (a) a substrate, (b) a circuit element situated in or over the substrate, and (c) an insulating layer situated over the circuit element and the substrate, the opening in the structure comprising an opening in the insulating layer, the opening in the insulating layer comprising a trench at least 2 μm long;

the titanium nitride layer and the tungsten layer extend into the opening in the insulating layer; and

the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening in the insulating layer.

38. The method of claim **37** wherein the substrate is a semiconductor substrate.

39. The method of claim **38** wherein the trench is at least 1 mm long.

40. The method of claim **39** further comprising, before forming the titanium nitride layer, depositing a titanium layer over the insulating layer such that the titanium layer extends at least into an opening in the insulating layer and such that the tungsten layer electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening in the insulating layer.

41. The method of claim **40** wherein the trench does not penetrate the insulating layer but a via at the bottom of the trench penetrates the insulating layer and exposes the circuit element, wherein the titanium layer physically contacts the circuit element at the bottom of the via.

42. The method of claim **39** wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.

43. A structure formed by the method of claim **31**.

44. The structure of claim **43** wherein the titanium nitride layer has a substantially columnar grain structure.

45. The method of claim **31** where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

46. The method of claim **45** wherein the tungsten halide comprises tungsten hexafluoride.

47. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

48. The method of claim **47** wherein the titanium nitride layer is formed by sputtering.

49. The method of claim **47** further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

50. The method of claim **47** wherein the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

51. The method of claim **50** wherein the tungsten halide comprises tungsten hexafluoride.

52. A fabrication method comprising:

forming a titanium nitride layer over a structure by physical vapor deposition such that the titanium nitride layer extends at least into an opening in the structure, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening, the chemical vapor deposition of the tungsten layer comprising reacting a tungsten halide with silane and subsequently with hydrogen.

53. The method of claim **52** wherein the tungsten halide comprises tungsten hexafluoride.

54. The method of claim **52** wherein the titanium nitride layer is formed by sputtering.

* * * * *

EXHIBIT B

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Effects of Barrier-Metal Schemes of Tungsten Plugs and Blanket Film Deposition

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This work investigates the effects of various contact integration schemes on tungsten (W) plug formation. The deposition rate, surface morphology, sheet resistance and reflectivity of W deposited on various substrates are also characterized. Experimental results indicate that the titanium nitride (TiN) film which does not undergo post-rapid-thermal-processing (RTP) treatment has a higher W deposition rate than TiN film which under goes the post-RTP treatment. The W plug formed on chemical vapor deposition (CVD) TiN has easily found voids, which result in high contact resistance. To reveal the relationship of CVD TiN process conditions and W plug loss, process variables including film thickness, plasma ambient, *in situ* plasma treatment periods and cycles are tested. According to these results, plasma ambient has a strong influence on W plug loss during the etch-back process. In addition, the electrical characteristics of various contact integration schemes are examined in terms of both n^+ and p^+ contact resistance. This work also proposes a superior contact integration scheme to achieve low contact resistance and high production efficiency.

KEYWORDS: PVD TiN, CVD TiN, plasma, W plug, RTP

1. Introduction

As device dimensions shrink to the sub half-micron scale and below, the filling of a high aspect ratio contact hole or via is an inherent part of the design. In chemical vapor deposition (CVD), tungsten (W) has been extensively applied to contact/via plugs and interconnects owing to its superior step-coverage.[1–6] Generally, titanium nitride (TiN) film acts as an adhesive layer for W deposition and as a diffusion barrier which offers protection against the reaction of WF_6 and Ti.[7–10] The conformity of TiN film is essential and is a process challenge when fabricating deep holes with small features. Conventional physical vapor deposition (PVD) TiN film has been widely used as a barrier layer because of its high chemical stability and cleaner process than CVD process. However, obtaining acceptable step-coverage for a high aspect ratio hole is extremely difficult, because a serious overhang exists at the top corner of the hole and limits the subsequent filling of films, *e.g.*, CVD W and Al sputtering. Therefore, CVD TiN film is widely used because of its excellent step-coverage of trenches with an aspect ratio up to seven has been demonstrated.[11]

Various CVD TiN film formation methods have been reported.[12–15] Two widely used organometallics are tetrakis-dimethylamino-titanium (TDMAT), and tetrakis-diethylamino-titanium (TDEAT). The incorporation of carbon is a problem which arises in the synthetic method. Oxygen which is absorbed into as-deposited TiN films increase film resistivity and is another processing problem. To solve these problems, related investigations have employed *in situ* plasma treatment in order to reduce the carbon content and increase film stability.[16,17]

Other investigations have presented various barrier-metal schemes, including ionized metal plasma (IMP) Ti/RTP/PVD TiN, IMP Ti/RTP/CVD TiN, IMP Ti/PVD TiN/RTP, IMP Ti/CVD TiN/RTP.[18,19] Using CVD TiN film as the barrier layer for W deposition is generally found to cause serious W plug loss problems during W etch-back.[20] Several methods, such as capping a PVD TiN film on a CVD TiN film, or reducing the etching rate have been used. However, these methods are not efficient for production. Enhancing CVD TiN film stability rather than optimizing the W etch-back process procedure is the preferred approach since the tunable process parameters of etch-back are found to be too narrow in the present study.

This work elucidates the physical properties of W deposited on various substrates. The film properties of CVD TiN and PVD TiN are studied. Here, the CVD TiN film is based on the thermal decomposition of TDMAT. Scanning electron microscope (SEM) is used to inspect W plug contacts formed by different contact integration schemes, including various types of TiN films and RTP process sequences, and the contact resistance of n^+ and p^+ are evaluated in the dynamic random access memory (DRAM) product.

2. Experimental

PVD TiN film, IMP Ti film and CVD TiN film were fabricated in either PVD or CVD chamber of Applied Materials Endura systems, and RTP and CVD W film were conducted in lamp-heat and CVD chamber of Applied Materials Centura systems, respectively. IMP Ti film deposition was performed at a temperature of 300°C, and PVD TiN film deposition was carried out in an unheated chamber with a collimator inserted for enhanced film step-coverage. CVD TiN film was deposited using TDMAT with or without *in situ* plasma treatment at a temperature of 450°C and with helium (He) as the delivering gas. *In situ* plasma treatments were conducted using N_2 or N_2/H_2, which was following the as-deposited film in the same chamber. In this study, the cycle was carried out one or twice, and the treatment period was 30 s or 60 s. One cycle indicates film deposited by one plasma treatment, and two cycles refers to the repetition of one cycle. This study uses "cycle *x* thickness" to denote the deposition condition of film. The RTP process was conducted in NH_3 ambient with two process temperature and period steps, which were 600°C, 60 s and 760°C, 20 s. W films were deposited by reducing WF_6 with hydrogen at a heater temperature of 450°C. Followed by

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Table I. Samples 1 to 20 with the following contact integration schemes are deposited on Si (100), structure or device wafers. The thickness of IMP Ti = 600 Å and the RTP conditions are 600°C, 60 s, 760°C, 20 s in NH_3 ambient; the barriers films using either PVD or CVD TiN are found as follows. CVD TiN plasma-treatment period is 30 s for one cycle except for sample 8, which is 60 s for one cycle.

Sample no.	Barrier film condition	Contact integration scheme	Types of wafer
1;11;16	PVD TiN = 600 Å	IMP Ti/RTP/PVD TiN/W	Si; structure; device
2;12;17	CVD TiN = 2 × 100 Å (N_2/H_2)	IMP Ti/RTP/CVD TiN/W	Si; structure; device
3;13;18	CVD TiN[a)] = 150 Å	IMP Ti/RTP/CVD TiN/W	Si; structure; device
4;14;19	CVD TiN[a)] = 150 Å	IMP Ti/CVD TiN/RTP/W	Si; structure; device
5;15;20	CVD TiN = 2 × 100 Å (N_2/H_2)	IMP Ti/CVD TiN/RTP/W	Si; structure; device
6	CVD TiN[a)] = 150 Å	IMP Ti/RTP/CVD TiN/W	structure
7	CVD TiN = 1 × 150 Å (N_2/H_2)	IMP Ti/RTP/CVD TiN/W	structure
8	CVD TiN = 1 × 150 Å (N_2/H_2)	IMP Ti/RTP/CVD TiN/W	structure
9	CVD TiN = 2 × 100 Å (N_2/H_2)	IMP Ti/RTP/CVD TiN/W	structure
10	CVD TiN = 2 × 100 Å (N_2)	IMP Ti/RTP/CVD TiN/W	structure

a) CVD TiN which did not undergo *in situ* plasma treatment.

blanket W deposition to a thickness of 5000 Å, the W etch-back step was implemented at a 40°C cathode temperature with a top electrode, and an RF source of 13.56 MHz was used. The etching process was conducted using SF_6 plasma with an *in situ* detecting fluorine signal. The endpoint was determined when significantly increased fluorine intensity was detected, which occurred during TiN film exposure and the following overetching time was set at 45 s.

The experiments were conducted on 8-inch Si (100) p-type wafers. Contact integration schemes listed in Table I were performed on a blanket Si (100) wafer, structure wafer with an aspect ratio (A.R.) of 7, 0.3 μm feature size and 0.3 μm 64 Mb DRAM. Physical properties of the W film, including the deposition rate, sheet resistance, and film resistivity were examined in blanket W deposited on various substrates. Electrical characteristics of contact resistance and leakage current were evaluated at 0.3 μm 64 Mb DRAM. Moreover, the surface morphology and film reflectivity of various barrier-metal combinations, as listed in Table II, are determined.

The film thickness was determined via fluorescent X-ray. The surface morphology was measured using an atomic force microscope (AFM) and the film reflectivity was determined by a opti-probe instrument. Four-point probes were used to measure the sheet resistance of W blanket films. Lastly, the cross section and top views of the W plugs were evaluated by SEM.

3. Experimental Results

3.1 Physical properties of tungsten on various substrates

To elucidate the dependence of barrier-metals on W film deposition, samples 1 to 5 listed in Table I were deposited on 8-inch blanket wafers, which mimic actual contact metal schemes. Only the barrier film of sample 1 is PVD TiN film formed by reactive sputtering in poisoned mode (i.e., the target is nitrided) as a standard for comparison with CVD TiN film, while the others are CVD TiN film. In order to elucidate the differences between the properties of W film deposited on CVD TiN film with and without plasma treatment, samples 2 and 5 are CVD TiN film (2 × 100 Å) and samples 3 and 4 are CVD TiN film which have not undergone *in situ* plasma treatment. Moreover, the RTP process sequence of the contact integration sequence is changed, either before or after TiN deposition, in order to understand the effect of RTP on W film deposition. Samples 1 to 3 are RTP processed before TiN film deposition, and samples 4 and 5 are RTP processed after. Figure 1(a) presents the W film thicknesses and average deposition rates for samples 1 to 5. The results indicate that the W deposition rate is higher for film deposited on CVD TiN film, and that the W deposition rate decreases if RTP is performed after barrier film deposition. A 1.6% decrease in the deposition rate is seen for sample 5 as compared to sample 2, and a 4% decrease is seen for sample 4 as compared to sample 3. This indicates that a higher rate of decrease is obtained for W film on CVD TiN film without *in situ* plasma treatment. Figure 1(b) illustrates the sheet resistances and resistivities of samples 1 to 5. The resistivity is derived by multiplying the sheet resistance by average W film thickness. Higher film resistivity is obtained when RTP is performed prior to barrier film deposition. In other words, W films have lower resistivity than barrier films which have undergone the post-RTP process. An 8.5% decrease in the film resistivity is seen for sample 5 as compared to sample 2, and an 11.5% decrease is seen for sample 4 as compared to sample 3. Furthermore, W films on CVD TiN film exhibit lower resisitivity compared with those on PVD TiN film. These results indicate that the properties of W film are related to the substrate conditions including the barrier film conditions and the RTP process sequence. Barrier film using either the CVD or PVD method has different surface morphology and composition and may change if RTP is carried out. The effect of the RTP process sequence on CVD TiN film which did not undergo plasma

Table II. Samples 21 to 25 with the following contact integration schemes are deposited on Si (100) substrates. Process conditions of IMP Ti and RTP are the same as those shown in Table I and the CVD TiN *in situ* plasma-treatment period is 30 s for one cycle.

Sample no.	Barrier film condition	Scheme for tungsten deposition
21	PVD TiN = 600 Å	IMP Ti/RTP/PVD TiN
22	CVD TiN = 2 × 100 Å (N_2/H_2)	IMP Ti/RTP/CVD TiN
23	CVD TiN = 150 Å[a)]	IMP Ti/RTP/CVD TiN
24	CVD TiN = 150 Å[a)]	IMP Ti/CVD TiN/RTP
25	CVD TiN = 2 × 100 Å (N_2/H_2)	IMP Ti/CVD TiN/RTP

a) CVD TiN which did not undergo *in situ* plasma treatment.

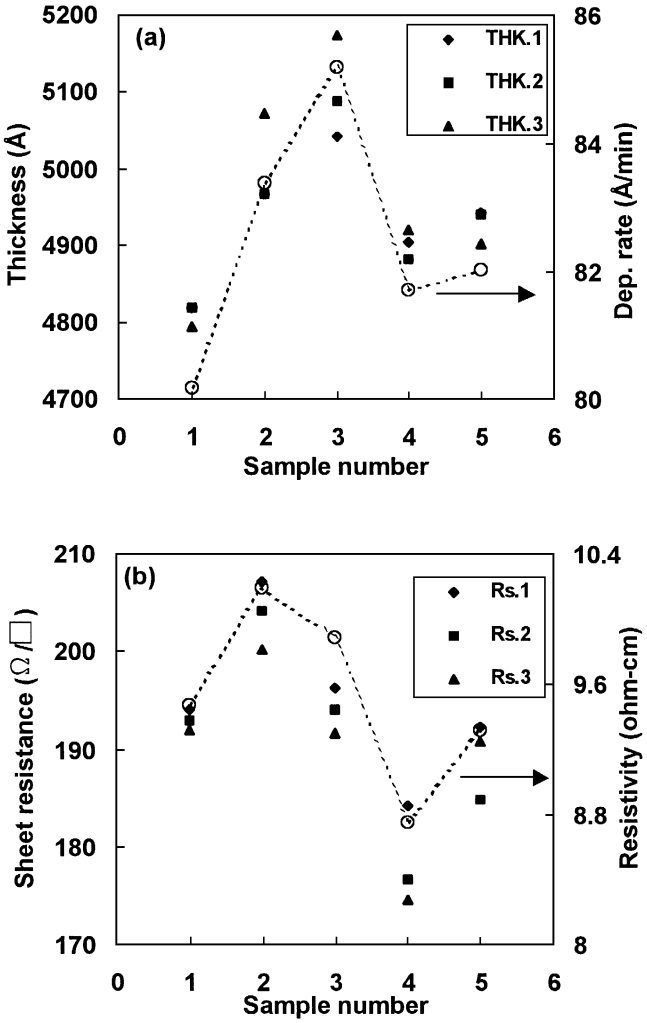

Fig. 1. Physical properties of tungsten deposited on samples 1 to 5 (a) thickness and average deposition rate of samples 1 to 5, (b) resistance and film resistivity of samples 1 to 5.

treatment is more pronounced than in that which underwent *in situ* plasma treatment according to the results for the film deposition rate and resistivity.

3.2 *Surface morphology and reflectivity*

To determine the top surface layer morphology of barrier film, we used AFM to examine the surface roughness of various barrier metals in a 5 μm × 5 μm region. Table II lists the conditions for samples 21 to 25, which are the corresponding schemes of samples 1 to 5 except in terms of W film deposition. Figure 2 presents the average surface root-mean square-roughness values (R_a) and reflectivity for samples 21 to 25. The film reflectivity is determined by the relative intensity of reflecting light for samples related to bare Si (i.e., intensity of sample/intensity of Si). In addition, the light wavelength used in this measurement is 465 nm. The surface roughness is related to the barrier-metal conditions. CVD TiN film which has undergone post-RTP treatment exhibits a lower R_a value corresponding to smoother surface morphology compared with that of CVD TiN which did not undergo post-RTP treatment. Results of W deposition rates show that it can be concluded the higher deposition rates are derived from rougher substrates, such as under the condition of RTP treatment before CVD TiN film deposition. In terms of film reflectivity, higher

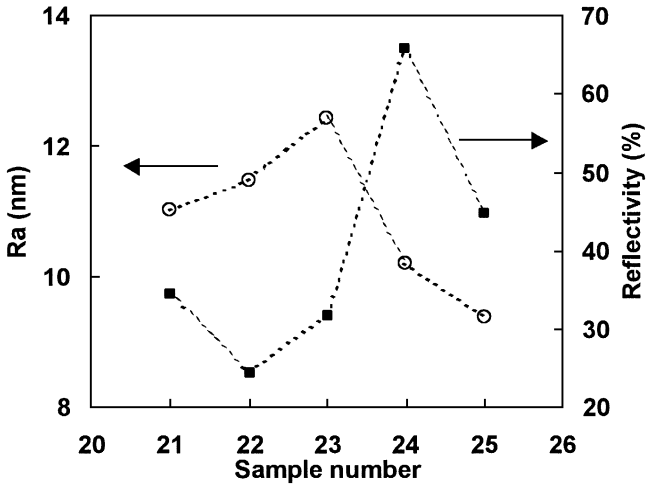

Fig. 2. Surface roughness determined by AFM and film reflectivity of samples 21 to 25.

values are obtained from samples 24 and 25 than from samples 21 to 23. Generally, higher film roughness corresponds to lower film reflectivity. However, the experimental results indicate that this relationship is inconsistent. Some factors, including film composition and structure, also influence film reflectivity, thus each sample may have a different film composition or structure.

3.3 *Contact metal schemes related to tungsten plug loss*

Figure 3(a) shows the schematic diagram of a structure

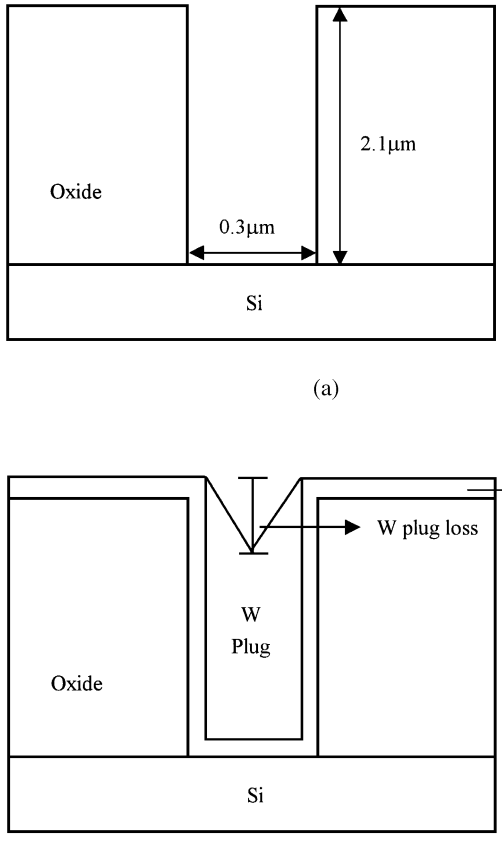

Fig. 3. Schematic representations of (a) cross-sectional view of structure wafer (b) measurement of W plug loss.

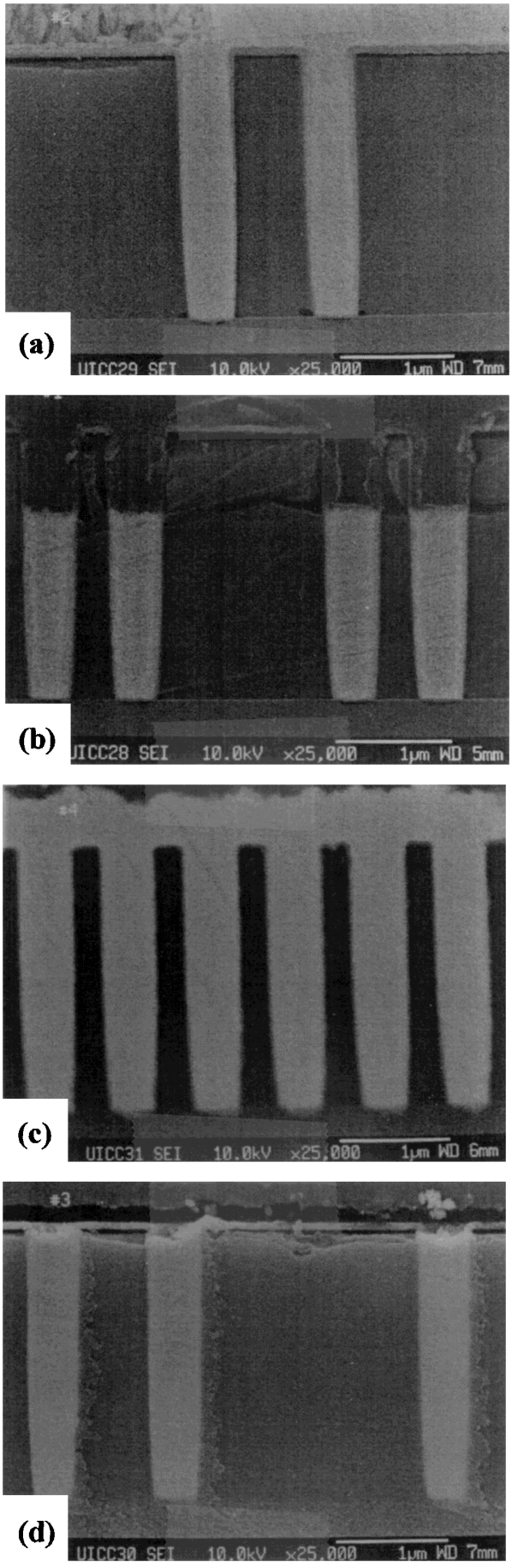

Fig. 4. W plug examined by CS-SEM. Results for sample 12 (a). Image of W plug evaluated before W etch-back (b). Image of W plug evaluated after W etch-back. Results for sample 15 (c). Image of W plug evaluated before W etch-back (d). Image of W plug evaluated after W etch-back.

wafer. Samples 11 to 15, which have the same contact integration schemes as samples 1 to 5, are processed in structure wafers. An IMP Ti film is applied as an adhesive layer; TiN film is used as a barrier layer and a seed layer for W film nucleation; blanket W film deposition followed by W etch-back is conducted to form a W plug. In this study, we measured the depth of W plug loss, as shown in Fig. 3(b), after W etch-back to determine the W plug quality. SEM inspections of samples 11 to 15 reveal that significant W plug loss is only found in sample 12, while the other samples are full W plugs. In order to determine whether the plug loss occurs during W deposition or W etch-back, we evaluated the W plug by cross-sectional SEM (CS-SEM) before and after W etch-back. Figures 4(a) and 4(b) present the CS-SEM micrographs of the W plug of sample 12 before and after W etch-back, respectively; Figures 4(c) and 4(d) show similarly obtained micrographs for sample 15. Significant W plug loss of approximately 6000 Å is evident in sample 12. However, a void-free W plug is found in sample 15.

These results indicate that W plug loss occurs during W etch-back; however, this could be prevented from altering the RTP process sequence. In our study of the W etch-back step, the etching stops when the TiN film is exposed. The etching selection between W and TiN film is a major factor governing plug integrity. CVD TiN film which has undergone post-RTP treatment is considered to improve etching selectively, and therefore the plug remains full after the W etch-back. Furthermore, CVD TiN films deposited with *in situ* plasma treatment in a deep hole have problems achieving good uniformity because of the anisotropic bombardment of plasma, which accentuates the subsequent W film nonuniformity. However, CVD TiN films which have undergone post-RTP treatment produce smoother surfaces with respect to R_a. Smoother or denser W films may be obtained for W deposited on these barrier layers, which have higher resistance to the W etch-back process.

To understand the various contact integration schemes in real devices, samples 16 to 20, with the same contact integration schemes as those of samples 1 to 5, are processed in a contact W plug of 0.3 μm 64 Mb DRAM, and the electrical characteristics of each sample are examined. Figure 5 presents the contact electrical characteristics of samples 16 to

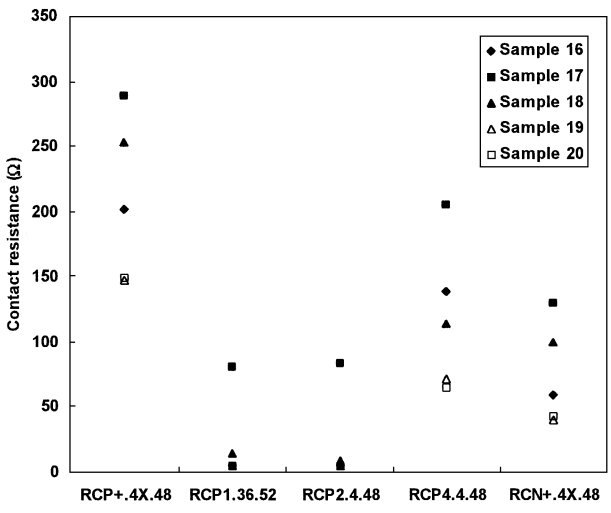

Fig. 5. Contact resistance of samples 16 to 20 evaluated at 0.3 μm 64 Mb DRAM.

20. R_c n^+ and R_c p^+ represent the resistance between the W plug and n^+ and p^+, respectively, and R_c P1 P2 and P4 represent the resistance between the W plug and each corresponding polysilicon line. Interestingly, the ranks of test sample contact resistance on device wafers are identical to the film resistivity of test samples on the W blanket wafers mentioned in §3.1. Apparently, a higher contact resistance is found in the RTP process sequence which occurs before TiN deposition than that of the post-RTP process sequence; thus, lower contact resistance is found in samples 19 and 20 than in sample 16, where the barrier film of samples 19 and 20 is CVD TiN and that of sample 16 is PVD TiN. The lowest R_c n^+ and R_c p^+ are processed in the sequence IMP Ti 600 Å/CVD TiN150 Å/RTP, where the CVD-TiN film does not undergo *in situ* plasma treatment. Lastly, the contact-induced leakage currents of all test samples are lower than 10^{-12} A.

3.4 CVD-TiN process conditions related to tungsten plug loss

Many researchers have reported that CVD TiN film which does not undergo *in situ* plasma treatment has high film resistivity.[16,17,21] High carbon contents from precursor sources and the continuing incorporation of oxygen into film upon exposure to air increase the impurity concentration, thus greatly increasing film resistivity. *In situ* plasma treatment with N_2 or N_2/H_2, which efficiently reduces film resistivity and lowers the carbon and oxygen content has been investigated.[16,17]

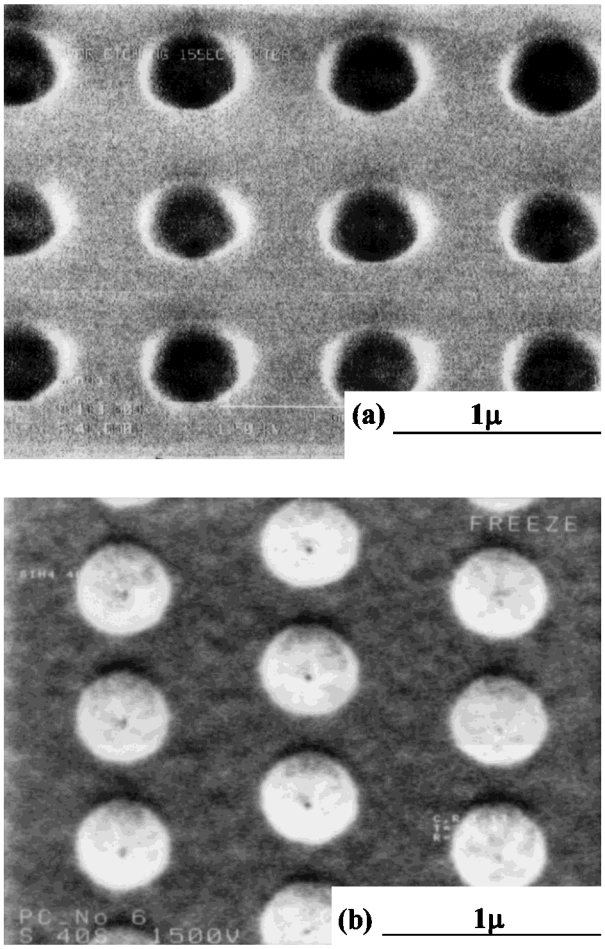

Fig. 6. W plug processed in structure wafer with T-SEM inspection. (a) sample 9, (b) sample 10.

As mentioned in §3.3, significant W plug loss appears in the contact integration scheme of IMP Ti/RTP/CVD TiN/W, where CVD TiN is 2 × 100 Å. In order to obtain a void-free W plug, process parameters including plasma-treatment period, cycles, and ambient are tested. We inspected the W plug by top-view SEM (T-SEM). The process conditions of samples 6 to 10 are indicated in Table I. The SEM inspections of samples 6 to 10 reveal that significant W plug loss is only found in sample 9, while the others are void-free W plugs. Figures 6(a) and 6(b) present the W plugs by T-SEM of samples 9 and 10, respectively. On the basis of SEM inspection, it can be concluded that the plasma-treatment ambient is the most important influential factor on film property. The W plug is not lost if W is deposited on CVD TiN film by plasma treatment in N_2 ambient, but significant loss occurs for W on CVD TiN film with treatment in N_2/H_2 ambient. In terms of film structure, CVD TiN film which does not undergo *in situ* plasma treatment is amorphous and the enhancement of film crystallinity via *in situ* plasma treatment is examined by X-ray diffraction;[16,22] different film crystallinities will be obtained if the cycle times of plasma treatment differ and CVD TiN films without any or with only one cycle of treatment gain more than twice the resistance of the W etch-back process. Moreover, different plasma-treatment ambiences may influence film composition; these details are currently being studied. The W plug is not lost in CVD TiN which does not undergo *in situ* plasma treatment. The existence of C and O impurities and amorphous films are considered to provide higher etching selectivity between W and TiN, and a more precise endpoint is detected in the W etch-back process.

4. Conclusions

This work has examined how contact integration schemes affect W film deposition. Contact integration schemes with low contact resistance were successfully designed through altering the RTP process sequence and the CVD TiN film process conditions. The key factor in obtaining a void-free W plug process is the employment of barrier-layer CVD/PVD TiN with post-RTP treatment. SEM results indicate significant W plug loss if the contact integration is IMP Ti/RTP/CVD TiN for CVD TiN (2 × 100 Å). However, the plasma-treatment ambient, cycle and periods were demonstrated to be able to tune the CVD TiN film properties and a void-free W plug could be realized by modifying the CVD TiN process. In commercial use, combining a PVD/CVD TiN chamber with a RTP chamber in the same instrument is not an ideal design, and a contact metal scheme such as IMP Ti/CVD TiN/RTP/W provides higher production efficiency.

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EXHIBIT C

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"Volcano" Reactions in Oxide Vias Between Tungsten CVD and Bias Sputtered TiN/Ti Films

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Tungsten chemical vapor deposition (CVD) remains the preferred method to make vertical metal interconnects in oxide vias on silicon integrated circuits. Vias are lined with thin titanium films, protected by a TiN diffusion barrier deposited on top followed by tungsten CVD. "Volcano" reactions, which result in rupture of the TiN barrier and electrical failure of the interconnect, remains an integration difficulty of great interest. Four parameters are found to strongly influence volcano reactions: the mixture of WF_6 and SiH_4 gases during tungsten nucleation film deposition, TiN barrier thickness, use of plasma preclean before Ti/TiN deposition, and a rapid thermal anneal after Ti/TiN deposition and before tungsten CVD. We describe process methods to avoid volcano reactions with thin TiN barrier films, maintaining low resistivity in the via. The influence of varying these parameters on overall step coverage is also discussed.

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Chemical vapor deposition (CVD) of tungsten is the preferred method to fill vertical interconnects (also called vias or plugs) between levels of metallization in silicon integrated circuits. The inability of sputter deposition to fill vias with high aspect ratios (depth to diameter) at low deposition temperatures has led to the widespread use of tungsten CVD, despite the higher resistivity of tungsten relative to aluminum or copper. The most commonly used tungsten CVD precursor molecule for silicon integrated circuits is tungsten hexafluoride, WF_6. Tungsten hexafluoride is a liquid at room temperature, unlike other precursors like WCl_6 and $W(CO)_6$, which are solids at room temperature.[1] Tungsten hexafluoride is a relatively simple molecule compared to other precursor molecules used in the semiconductor industry, like tetrakis(dimethylamido)-titanium (TDMAT) for TiN or dimethylaluminum hydride (DMAH) for aluminum, and is readily dissociated by H_2 at low temperatures. Two drawbacks of using WF_6 are difficulty in nucleating tungsten on TiN diffusion barriers and the corrosive fluorine byproduct. The first problem has been sidestepped by using SiH_4 to reduce WF_6, producing a thin, continuous tungsten nucleation film on TiN.[2] Further tungsten deposition is accomplished by H_2 reduction of WF_6 on the tungsten nucleation film. Deposition of tungsten by SiH_4 reduction of WF_6 on TiN occurs without an "incubation time," or time to initiate deposition, unlike H_2 reduction of WF_6 on TiN. Step coverage and deposition rate of tungsten films deposited by SiH_4 reduction of WF_6 are reduced compared to H_2 reduction, and are discussed. The second problem, fluorine contamination, has proven less tractable. Incorporation of fluorine in the tungsten film raises its resistivity.[3] A more serious problem is fluorine's penetration through the TiN diffusion barrier and into the titanium film.

Titanium films are deposited on highly doped regions of silicon to form $TiSi_2$ ohmic contacts upon subsequent annealing. When aluminum is used for horizontal interconnects, a thin titanium film is sometimes deposited on top prior to making a vertical connection to it. The titanium film reduces the oxide that forms on top of aluminum in between processing steps, maintaining lower resistance in the interconnect. Titanium can be attacked by WF_6 when a tungsten interconnect is deposited on it. Diffusion barrier films like TiN are employed to prevent reactions between WF_6 and titanium. Even with the use of TiN, fluorine has been shown to diffuse into the underlying titanium film.[4] At best, soluble fluorine in titanium merely raises its resistivity. At worst, fluorine can diffuse into the titanium to such a level to form TiF_x compounds.[5] Titanium fluoride (TiF_x), with high resistivity and stress from the volume expansion, forms readily when the solid solubility of fluorine in titanium is exceeded, and is an unwelcome addition to any film stack. Gaseous TiF_4 can also form.[5] The volume expansion of TiF_x formation can rupture the overlaying TiN film, resulting in greater WF_6 attack of the now exposed titanium film. When this happens in a via, the subsequent tungsten deposition on uplifted TiN results in a volcano-shaped amalgam of material above the via. These features yield defects upon subsequent dry etching or chemical mechanical polishing (CMP) to remove the blanket tungsten film.[6] The via fails electrically, and this failure has been dubbed the "volcano reaction."[7-9] While the basic mechanism of the failure, penetration of excess byproduct fluorine into the contact titanium film to form TiF_x, has been elucidated, the factors that influence the reaction have not. Immediate "fixes" to avoid volcano formation, such as increasing the thickness of the TiN diffusion barrier, often come with the penalty of increased resistance in the via. A better understanding of the factors that influence volcano formation may allow avoidance without a penalty in device performance.

In this paper, we define some of the parameters that influence the appearance of volcanoes in vias lined with Ti/TiN films deposited by biased sputtering. While sputtering has proven a cost effective method for depositing metal on silicon wafers, the inability of sputtering to achieve good step coverage in via and trench features with high aspect ratios has led to the use of CVD. CVD has much better step coverage in high aspect ratio features, although it is usually more costly than sputtering. Tungsten CVD is the most widely used technique to fill oxide vias for vertical interconnects in silicon. Since the liner/barrier films are typically much thinner than the diameter of the via, chip manufacturers have been slow to adopt CVD techniques for deposition of the liner/ barrier films, although this is changing. Use of high aspect ratio, deep vias by dynamic random access (DRAM) manufacturers has increased the need for improved step coverage of liner/barrier films.[10] Ionizing the sputtered metals and directing them normal to the wafer by applied bias provides a cost effective means to achieve adequate bottom coverage in vias with increasing aspect ratio. One method of achieving biased sputtering is by ionized metal plasma (IMP). The IMP process utilizes an inductively coupled plasma to ionize sputtered metal atoms, and the resulting metal ions are accelerated across the sheath by applying radio frequency (rf) bias. Highly directionalized ions are more effectively deposited on the bottom of vias.[11,12] The IMP process is used to deposit the TiN/Ti films in this set of experiments.

Several factors are found to influence volcano reaction: the use of a plasma preclean before liner/barrier film deposition, thickness of the barrier film, temperature of tungsten CVD, and the ratio of WF_6 to SiH_4 gas flow during nucleation film deposition. Consideration of these factors allows for a more complete description of the volcano reaction, and for an extension of current deposition techniques into higher aspect ratio vias with thinner barrier films. These parameters are intimately linked with the goal of achieving complete fill of vias

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with the minimal TiN thickness, and are discussed. A complete description of the parameters influencing the reaction, including the effects of film stress and via size/geometry, remains to be detailed. The paper is divided into two sections: volcano reactions in oxide vias with varying TiN barrier thickness and tungsten nucleation film gas flows, and step coverage in oxide vias. We find a close relationship between parameters influencing volcano reactions and the ability to achieve good step coverage.

Experimental

Titanium and titanium nitride deposition were accomplished by biased, IMP sputtering in an Applied Materials Vectra chamber. Conditions are summarized here, and a complete description is available in Ref. 11. The inductively coupled plasma had a density of $10^{11\text{-}12}/cm^3$. Direct current (dc) power is applied to the water cooled titanium target with a rotating magnet to create magnetron discharge to sputter the target. RF power is also applied to the coil inside the process cavity for ionization of metals. The source was operated at a relatively high pressure (15-30 mTorr) of argon (for titanium) or Ar + N_2 (for TiN), increasing the probability of ionization of the sputtered metal atoms. The metal ions are accelerated across the sheath by capacitively coupling the additional rf power (13.56 MHz) to the substrate pedestal. A plasma preclean was done on one set of wafers prior to titanium and TiN deposition. The preclean etched 300 Å of SiO_2 by placing the wafer in a chamber of 0.5 mTorr with 5 standard cubic centimeters per minute (sccm) argon and striking a plasma of 300 W.

Tungsten depositions, were carried out in an Applied Materials Centura 5200 WxZ cold walled, single wafer chamber with a resistively heated substrate. Reactive and inert gases were distributed uniformly over the wafer through a perforated plate. Tungsten deposition were preceded by depositing a monolayer of silicon in a process described in Ref. 13. Tungsten nucleation films were deposited at a pressure of 30 Torr with SiH_4 and WF_6 gases diluted in argon and H_2. After a 350 Å nucleation film was deposited, pressure in the chamber was increased to 90 Torr, and 95 sccm of WF_6 was reduced by 700 sccm of H_2, diluted in argon for a total film thickness of 3800 Å. The wafer susceptor temperature was either 425 or 375°C.

Wafers with 1.2 μm silicon dioxide film were etched with vias to silicon, with via diameters at the surface ranging from 0.25 to 0.6 μm. Via wafers were examined by scanning electron microscopy (SEM) on fractured cross sections and by transmission electron microscopy (TEM). Fluorine depth profiling through W/TiN/Ti film stacks was done by secondary ion mass spectrometry (SIMS). Sputtering for SIMS was done with 2 keV Cs^+ beam. Relative sensitivity factors for SIMS of fluorine in each matrix were determined from analyzing films of sputtered tungsten, titanium, and TiN, (each film on a separate oxide wafer), with fluorine ions implanted to a known dose. To minimize SIMS depth profile artifacts arising from initially rough surfaces and from sputter-induced roughening, tungsten films were treated by CMP to remove tungsten film and smooth the rough as-deposited surface.[14,15] Stress in the deposited films was determined by measuring wafer bow in a Tencor FLX-5200H before and after film deposition. Sheet resistance was measured by four point probe on 49 areas of the wafer. Resistivity of the films was extracted from sheet resistance measurements of the substrate and film. Rapid thermal anneals (RTAs) of TiN films were done in an Applied Materials Centura Radiance too at 580°C for 45 s in an N_2 ambient.

Results

Via Wafers and Volcanoes

It has recently been shown that pretreating metallorganic CVD TiN, particularly undense amorphous TiN, with SiH_4 under conditions that result in a silicon deposition to a concentration of $1.5 \times 10^{15}/cm^2$, or approximately a monolayer on TiN, results in a more homogeneous tungsten nucleation than without a SiH_4 pretreatment.[13] A heterogeneous nucleation, in which tungsten is deposited as discontinuous islands on TiN, lengthens the time to achieve continuous tungsten film coverage. A longer time to achieve continuous coverage increases exposure to WF_6. It has recently been shown that tungsten films are a much stronger barrier to fluorine penetration into underlying titanium films than TiN, making it imperative to achieve a continuous tungsten film as early as possible in deposition.[16] Therefore, all wafers in this experiment were pretreated with SiH_4 with conditions that produced a monolayer of silicon on the TiN surface prior to tungsten CVD. Wafers with vias were deposited with IMP Ti/TiN with two parameters: (*i*) with and without plasma preclean prior to Ti/TiN deposition, and (*ii*) with and without an RTA after Ti/TiN deposition. Tungsten CVD was performed at a wafer susceptor temperature of either 425 or 375°C. Table I summarizes each set of deposition conditions.

Table I. Process conditions for patterned wafers.

Set	Plasma preclean	RTA after TiN?	Tungsten CVD temperature (°C)
I	no	no	425°C
II	no	yes	425°C
III	yes	no	425°C
IV	no	yes	375°C

The volcano shape comes from the rupture of the TiN at the top edge of the via, with continued tungsten deposition forming the cone (Fig. 1). The Ti/TiN films are much thinner on the surface edge and sidewalls relative to the top surface outside the via and the bottom of the via. TEM micrographs (Fig. 2) show a fracture in the TiN film at the top edge of the via. As described previously,[9] the fracture occurs when fluorine indiffusion reaches a level at which TiF_x compounds form. The volume expansion causes a break in the TiN film, exposing further titanium to attack by WF_6. Bare titanium exposed to WF_6 rapidly forms TiF_x compounds.[5]

We study volcano formation on patterned wafers with consistent process conditions. By processing the wafers in the same deposition chambers and changing only one parameter, we are able to map the process window for volcano occurrence accurately and repeatably. All via wafers were deposited with 250 Å of titanium by the IMP process and various thicknesses of IMP TiN. Tungsten CVD was done with variations in the reactive gases during the nucleation film deposition: either 30 sccm WF_6 + 30 sccm SiH_4 (1:1 ratio), 45 sccm WF_6 + 30 sccm SiH_4 (3:2 ratio), 60 sccm WF_6 + 30 sccm SiH_4 (2:1 ratio), or 60 sccm WF_6 + 20 sccm SiH_4 (3:1 ratio). The nucleation gases were diluted in 2500 sccm of argon and 1000 sccm of H_2. It has been shown that when the gas flow of SiH_4 exceeds WF_6, silicon is incorporated into the tungsten film. Incorporation of silicon into tungsten increases the resistivity of the film, decreases the density, and results in poor step coverage.[17] Therefore, this deposition regime (SiH_4 flow > WF_6

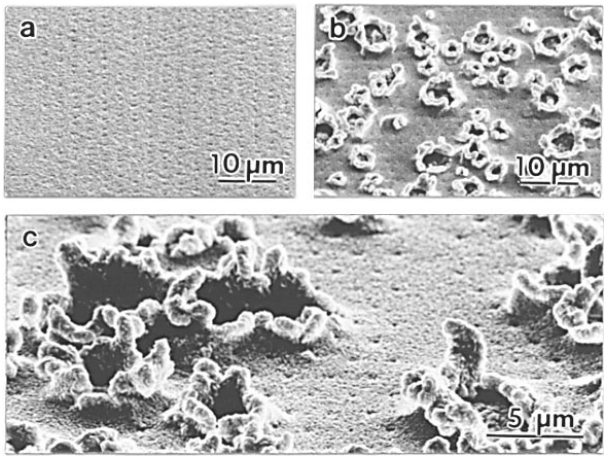

Figure 1. Top view of tungsten films on TiN/Ti/SiO_2 films with vias etched: (a) no volcanoes, the slight depressions in the tungsten film indicate a via beneath, (b) volcanoes, and (c) close-up of volcanoes. Images a and b are viewed 30° off normal, and image c is viewed 60° off normal.

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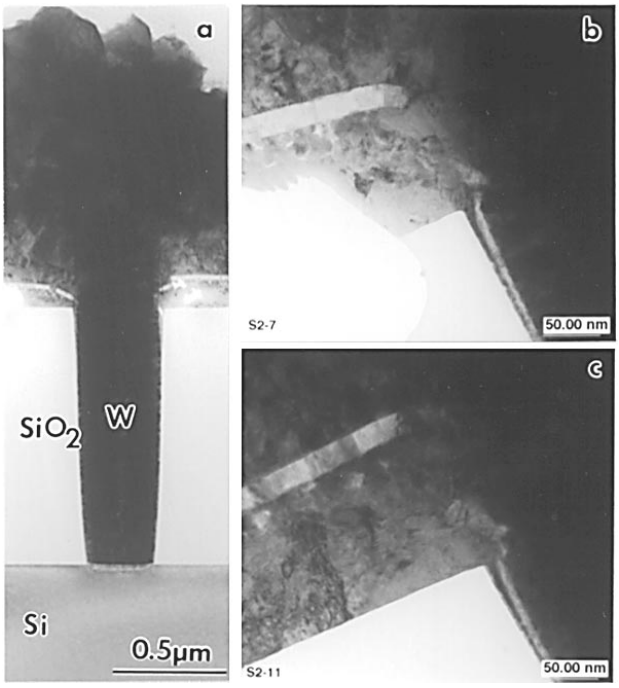

Figure 2. TEM micrographs of vias with volcanoes: (a) overall view of a failed via, (b) and (c) details of the failure at the fracture at the top corner of the via.

flow) was not investigated. Slightly different deposition rates were observed with different gas ratios, so the deposition time was adjusted to produce the same 350 Å nucleation film on each wafer. The bulk film depositions were the same on all wafers to provide a total film thickness of 3800 Å. We first summarize the results for each condition and then discuss the relationships between conditions.

The plot in Fig. 3 describes the occurrence of volcanoes for the wafers in set I (Table I). A wafer was considered to have failed if more than three volcano features were observed by SEM per via field, with each via field having over 10,000 vias. While this criterion is severe, most of the wafers that failed had far more than that. Figure 3 indicates the relationship between TiN film thickness and gas flow ratios that become more apparent in the following sets. The process conditions in set I had the greatest severity volcano formation of the four sets studied.

Figure 4 shows the results on via wafers that had an RTA after TiN deposition (set II). The RTA clearly allowed the use of thinner TiN for

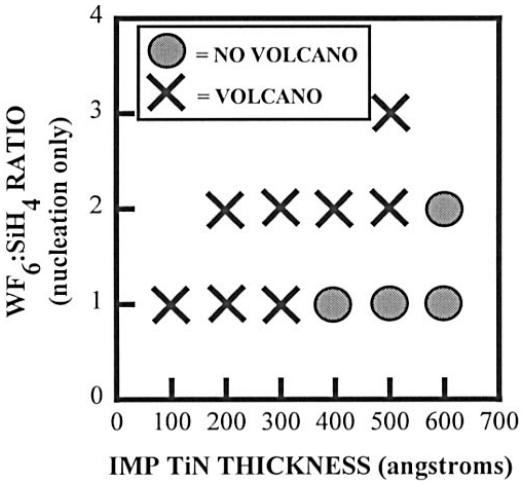

Figure 3. Volcano occurrence with TiN thickness and WF_6:SiH_4 ratio for set I wafers (no plasma preclean, no RTA after Ti/TiN deposition). Tungsten CVD at 425°C.

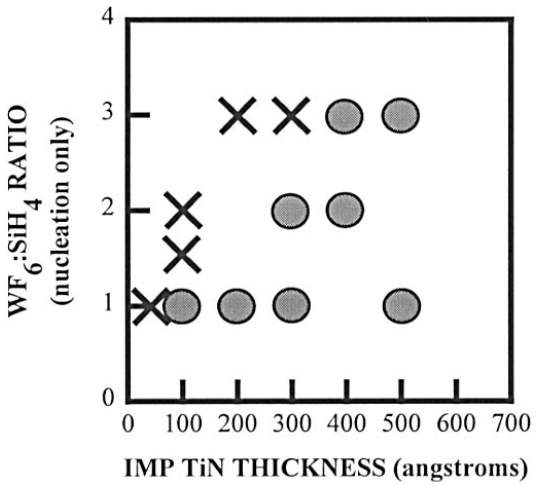

Figure 4. Volcano occurrence with TiN thickness and WF_6:SiH_4 ratio for set II wafers (no plasma preclean, RTA after Ti/tiN deposition). Tungsten CVD at 425°C.

several gas ratio conditions that had produced volcanoes in set I above. It has been speculated that the RTA "cures" the TiN of pinhole defects.[9] Pinholes provide a facile path for WF_6 to diffuse to the titanium film, accelerating volcano formation. An RTA is executed at contact level after Ti/TiN deposition. The RTA transforms the titanium to C54 $TiSi_2$ to form an ohmic contact to highly doped regions. These silicidation anneals are done at 700-800°C for ~60 s. However, an RTA is often not possible for metallization subsequent to the contact level because of the use of aluminum (low melting point) for upper level interconnects. It is apparent that higher WF_6:SiH_4 gas flow ratios can be used only with thicker TiN films in set II. In both sets I and II, the thinnest TiN barrier that prevented volcano formation was achieved with a 1:1 WF_6 to SiH_4 gas flow ratio. For a 1:1 ratio of WF_6 to SiH_4, TiN can be 100 Å with an RTA, whereas in set I, a minimum of 400 Å was needed to avoid the volcano reaction.

A plasma preclean removes the native oxide on Si surface prior to deposition of Ti. The oxide is detrimental to device performance. The preclean removes ~300 Å of SiO_2 in the thick film used to insulate the vias and results in the corners at the via entrance being "rounded"; this is discussed in the Step Coverage section. Figure 5 shows the results on via wafers that have had a plasma preclean prior to Ti/TiN deposition (set III). The preclean has an even more beneficial influence than the RTA: TiN as thin as 50 Å can prevent the volcano reaction for gas ratios of 1:1. A 2:1 gas ratio can be used with 100 Å TiN, impossible with only an RTA on the TiN.

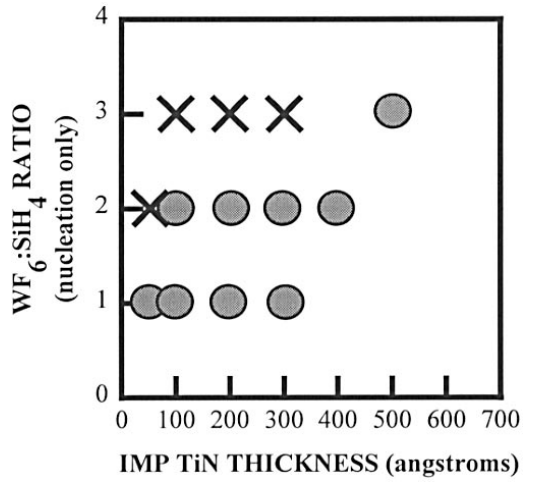

Figure 5. Volcano occurrence with TiN thickness and WF_6:SiH_4 ratio for set III wafers (plasma preclean, no RTA after Ti/TiN deposition). Tungsten CVD at 425°C.

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The thermal budget for "back end" processes is decreasing due to the use of thermally sensitive dielectrics materials, and to achieve improved step coverage in vias. Step coverage for tungsten CVD improves for high aspect ratio (HAR) vias (higher than those studied here) with lower deposition temperatures, but also increases the stress in the tungsten film, and decreases the deposition rate. The nucleation film deposition time goes from 11 s for a 1:1 gas ratio at 425°C, to 14 s at 375°C to produce a 350 Å film. Deposition rate by H_2 reduction in the second step is more sensitive to temperature: deposition time doubles to 154 s from 75 s to deposit 3450 Å. While 100 Å TiN is still compatible with 1:1 nucleation films at 375°C tungsten CVD temperature, higher gas ratios can no longer be used with thicker TiN films, as was the case with tungsten CVD at 425°C (Fig. 6). Set IV is identical to set III except for the lower tungsten deposition temperature. The process window for volcano avoidance is clearly smaller at lower temperatures.

The plots in Fig. 3, 4, 5, and 6 show the beneficial effect of thicker TiN films for avoiding volcanoes. We expect that thicker TiN will allow less fluorine penetration. To illuminate the difference in fluorine penetration with TiN thickness and gas ratio in the nucleation film, fluorine was depth profiled by SIMS. Tungsten was deposited at 425°C using a 3:1 ratio on substrates with 1000 Å IMP titanium and either 100 or 400 Å IMP TiN that had received an RTA (similar to set II above). Figures 7a and b show that thicker TiN allowed less fluorine penetration into the titanium. The fluorine dose in the titanium film is reduced by an order of magnitude when going from 100 to 400 Å TiN thickness, showing a thicker TiN film is, indeed, a better barrier (Table II). A previous estimate for the upper bound for fluorine diffusivity in tungsten, $D_F(W) = 4 \times 10^{-14}$ cm^2/s at a wafer susceptor[16] temperature of 425°C (wafer temperature ~415°C) allows for an estimate of fluorine diffusion length in tungsten with wafer time on the susceptor.[15] The total time the wafer is at temperature after initial exposure to WF_6 until a 3800 Å film is deposited and the wafer leaves the susceptor is ~100 s. This yields a diffusion length of ~200 Å for fluorine in tungsten. With a previous estimate of D_F (Ti) at 440°C of 10^{-12} cm^2/s, we can conclude that fluorine diffusion in tungsten is probably much slower than in titanium. This implies that the fluorine in TiN/Ti arises from initial exposure of the TiN to WF_6 and the nucleation film deposition, but not bulk film deposition. While there is a high concentration of fluorine in the tungsten film, 3×10^{19}/cm^3, its slow diffusivity does not allow the vast majority of it to reach the titanium film. However, the cumulative effect of subsequent thermal cycles, especially for integrated circuits with multiple layers of metallization may continue to increase the fluorine level in the titanium film. Subsequent thermal cycling is not addressed in the current work.

The dependence of fluorine penetration with WF_6:SiH_4 ratio is shown in Fig. 7b and c. The fluorine depth profile in a film stack of tungsten CVD/100 Å TiN (RTA)/1000 Å IMP titanium/oxide with a 30:30 flow ratio *vs.* a 60:20 WF_6:SiH_4 flow shows that the titanium film has a fluorine dose in the 30:30 sample that is one-quarter of the level in the 60:20 sample (Table II). This correlates well with the volcano plots in Fig. 3, 4, 5, and 6. A lower level of fluorine is also evident in the tungsten nucleation film in Fig. 7c; the fluorine level drops

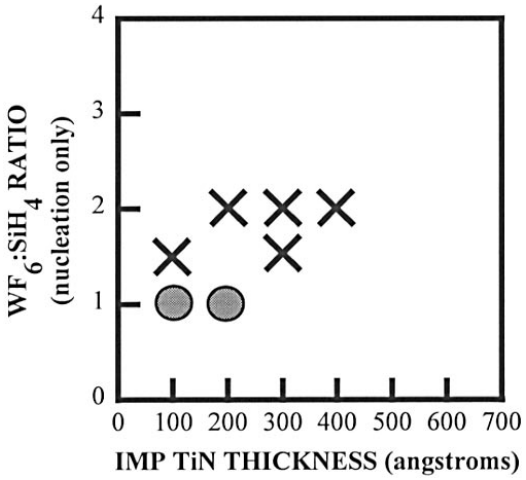

Figure 6. Volcano occurrence with TiN thickness and WF_6:SiH_4 ratio for set IV (no plasma preclean, RTA after Ti/TiN deposition). Tungsten CVD at 375°C.

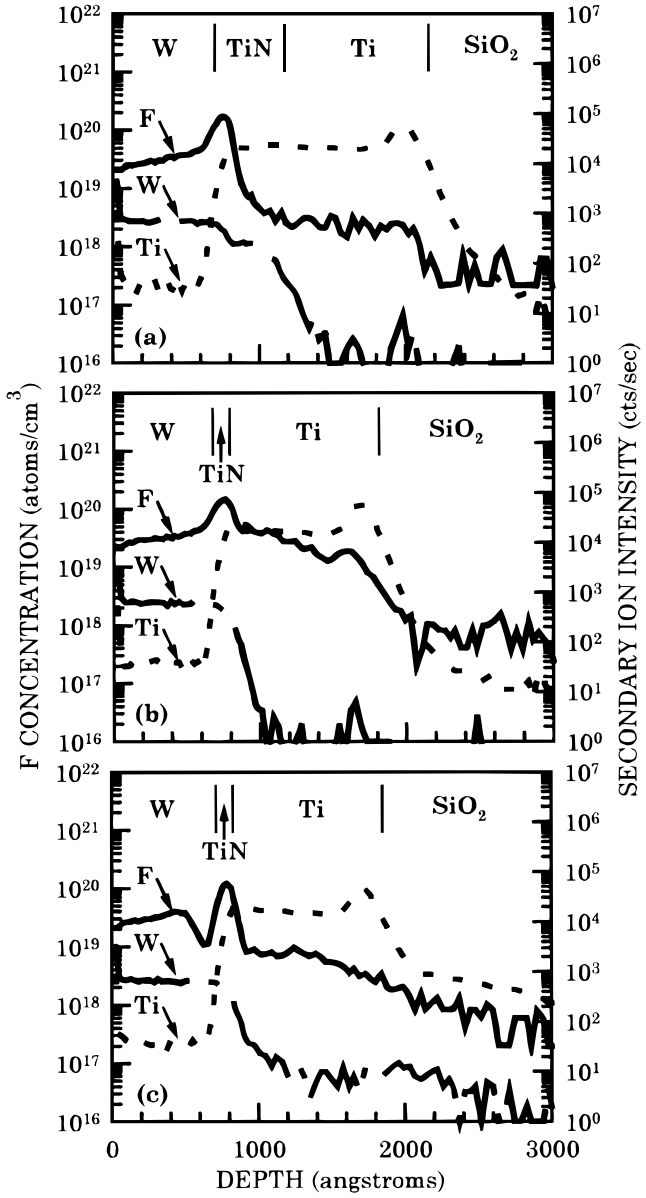

Figure 7. SIMS depth profile of fluorine through film stacks of tungsten CVD/TiN/Ti. Process conditions: (a) tungsten CVD 425°C with 60:20 ratio/400 Å TiN (RTA)/1000 Å Ti/oxide, (b) tungsten CVD 425°C with 60:20 ratio/100 Å TiN (RTA)/1000 Å Ti/oxide, and (c) tungsten CVD 425°C with 30:30 ratio/100 Å TiN (RTA)/1000 Å Ti/oxide.

Table II. Fluorine dose in the titanium film (1000 Å on oxide) with various process conditions.

TiN thickness (Å)	RTA after TiN?	WF_6:SiH_4 flow (sccm)	Tungsten CVD temperature (°C)	F dose in Ti ($\times 10^{13}$/cm^2)
400	yes	60:20	425	2
100	yes	60:20	425	20
100	yes	30:30	425	5

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from $\sim 3 \times 10^{19}/cm^3$ from the H_2 reduced WF_6 film to $1 \times 10^{19}/cm^3$ in the 30:30 nucleation film. This also belies the relatively slow diffusivity of fluorine in tungsten. While the fluorine levels in these flat film wafers (no patterning) is not sufficient to produce TiF_x, the amount of TiN/Ti that gets deposited on the via sidewalls is much less than on the flat surfaces. The step coverage of the IMP TiN is approximately 10% on the sidewalls, so for a 100 Å TiN film deposition, the TiN on the sidewalls is only 10 Å. The titanium film has similar step coverage. Accurate SIMS depth profiling for very thin films such as this is not possible. We use the thick TiN films in Fig. 7 as indications of relative fluorine levels in the film stacks in the vias themselves.

The plots of volcano occurrence and SIMS show that fluorine penetration is increased with the partial pressure of WF_6. The partial pressure for 60 sccm of WF_6 is twice that for a 30 sccm flow for the tungsten deposition conditions in this set of experiments. Increasing the partial pressure of WF_6 increases the rate of both TiF_3 and TiF_4 formation. The fact that for 300 Å TiN barrier film with tungsten nucleation 60:30 gas flow ratio did not produce a volcano while a 60:20 ratio did, indicates an additional factor for volcano formation: "naked" WF_6 flow. Naked WF_6 flow is defined as (WF_6 flow) − (SiH_4 flow). The partial pressure of WF_6 is the same, only SiH_4 partial pressure is reduced. In this case, it is apparent that both a higher partial pressure of WF_6 and higher amount of naked WF_6 increase volcano occurrence.

The process by which SiH_4 breaks up WF_6 and fluorine is removed has been explored by Kabayashi *et al*.[18] with reactive gases diluted in N_2. When WF_6 breaks on the TiN tungsten surface, some fraction of fluorine or fluorine compound is incorporated into the growing tungsten film and diffuses to the TiN, although the vast majority is removed from the deposition chamber. The amount in the film stack increases with the partial pressure of WF_6 and amount of naked WF_6. This implies that when the amount of SiH_4 flow is decreased while WF_6 is not (*e.g.*, a 60:20 ratio *vs*. a 60:30 ratio), the WF_6 dissociation products are not removed from the growing film as efficiently.

For the four sets of conditions studied with oxide via wafers, those wafers that received a plasma preclean clearly had the widest process window, allowing the use of thin TiN barriers and/or high WF_6:SiH_4 gas flow ratios. The large benefit of the plasma preclean for avoiding volcano formation was unexpected. The rounding of sharp corners at the surface of the via minimizes the severity of the reentrant profile of the TiN/Ti films, and minimizes the local stress buildup in that area that develops during subsequent thermal cycling. A reentrant profile describes the decreasing film thickness from the surface of the via to the sidewalls. The actual failure of the TiN films was observed to appear at the top corner of the via (Fig. 1 and 2). Film stress may play a role in the narrowing of the process window for volcano occurrence for tungsten CVD done at 375°C, and in the RTA's beneficial effect on reducing volcano occurrence. Fluorine depth profile in the film stack [tungsten CVD (30:30)/100 Å TiN (RTA)/1000 Å Ti/oxide] with tungsten deposition at 375°C was, surprisingly, little different from Fig. 7c (same conditions but with tungsten CVD at 425°C). Although no measurement of fluorine diffusivities at temperatures below those already mentioned could be found, we expect that the diffusivity will decline with temperature. It is possible that the lower fluorine diffusivity at 375°C was compensated by the longer deposition time needed to produce the same thickness film, allowing for near equivalent fluorine diffusion lengths. The measured stress in 3800 Å tungsten films was 1.5×10^{10} tensile dyn/cm^2 for the deposition at 425°C *vs*. 1.8×10^{10} tensile dyn/cm^2 for the deposition at 375°C. The increased tensile stress in tungsten deposited at lower temperatures may act adversely on the TiN, increasing the likelihood of a fracture and volcanoes. A higher pre-existing tensile stress in the TiN would make its fracture easier when TiF_x grows and expands underneath. Stress is measured to decline from 3×10^{10} dyn/cm^2 compressive to 1.5×10^{10} dyn/cm^2 compressive in 300 Å IMP TiN films on 250 Å IMP Ti/oxide on wafers without patterning after an RTA. This reduction in TiN stress may be the cause of the improved volcano resistance after an RTA. The RTA may strengthen the TiN resistance to volcano reaction by densification; Ramanath *et al*. found WF_6 diffused through "annular nanopipes" in sputtered TiN, with WF_6 breaking up deep within the TiN or even at the TiN/Ti interface, allowing WF_6 and WF_6 byproducts to diffuse more quickly into the titanium.[4] Deconvoluting parameters such as film stress reduction and TiN densification that influence volcano occurrence is difficult. A SIMS depth profile of the film stack tungsten CVD (30:30)/100 Å TiN (no RTA)/1000 Å IMP Ti/oxide film shows little difference from that of Fig. 7c, in which the TiN has received an RTA implying that the film stress does play a role in volcano formation. However, depth profile resolution may not have allowed fine differences to be evident. Fluorine penetration differences like those in Fig. 7 were not visible with either an RTA of the TiN films or with decreasing tungsten deposition temperature to 375°C. There is no doubt from Fig. 3 and 4 that the RTA was beneficial in preventing the volcano reaction, while it was not apparent from the SIMS depth profile that fluorine penetration into the TiN/Ti film was reduced after the RTA.

Step Coverage

High step coverage of all the films in the via is important for two reasons: (*i*) overall via resistance increases when vacuum is substituted for metal, and (*ii*) if the wafer is chemical mechanically polished after tungsten deposition and a "seam" or "keyhole" exists in the via, as in Fig. 8b, the seam may become open to the surface after CMP, and the corrosive slurry used in CMP can degrade the quality of the via. Seams or keyholes such as that Fig. 8b are undesirable.

Step coverage is determined by measuring the thickness of the W/TiN/Ti film stack on the sidewall at mid depth and dividing by one half the diameter of the via at the oxide surface. The bowed profile of the via, in which the diameter at middepth is somewhat larger than at either the oxide surface or bottom of the via, makes it impossible to completely fill the via without a keyhole. Nucleation film step coverage is about 70% for the 30:30 gas flow ratio (Fig. 9). By comparing the via diameter at the oxide surface after TiN deposition, tungsten nucleation film deposition and complete fill of the via with tungsten, we can conclude that H_2 reduction of WF_6 results in near 100% step coverage. While the nucleation film thickness was held constant at 350 Å in this study, the use of thinner nucleation films can improve overall step coverage (provided that the nucleation film is continuous). Study of how nucleation film thickness affects overall tungsten step coverage was not pursued in this work.

Step coverage is largely affected by the thickness of the TiN film. Overall step coverage is shown *vs*. thickness of the TiN film (Fig. 10). The nonconformal TiN step coverage at the surface edge of the via (reentrant profile) is largely responsible for the decreasing tungsten film step coverage with increased TiN/Ti thickness (Fig. 8c), and has been discussed extensively elsewhere.[12] It is important to note that the IMP process minimizes the overhang at the top surface edge of the via: unbiased sputtering would produce a more severe overhang.

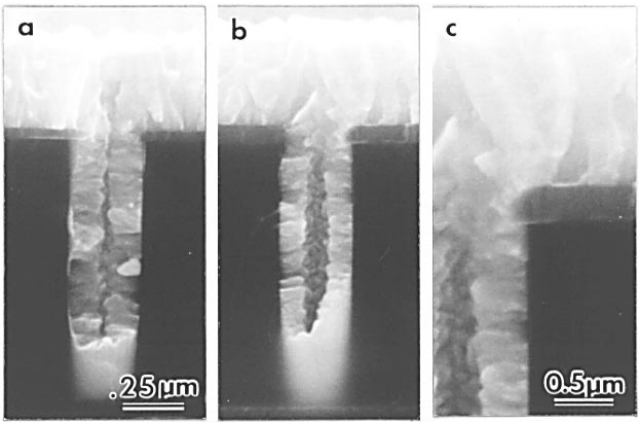

Figure 8. SEM micrographs of oxide via filled with tungsten CVD/TiN/250 Å with an RTA (set II): (a) 100 Å TiN, (b) 500 Å TiN, and (c) detail with 500 Å TiN.

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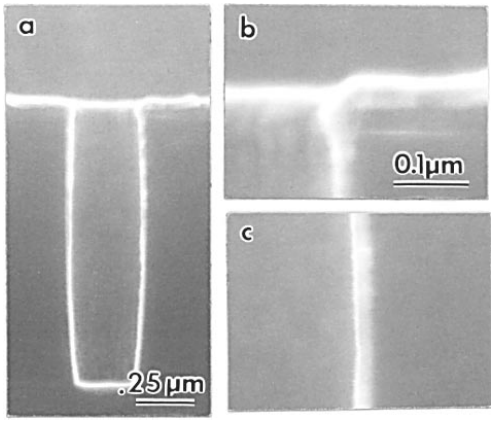

Figure 9. SEM micrographs of nucleation film step coverage in a via with WF_6:SiH_4 gas ratios of 30:30: (a) overall, (b) at the top corner, and (c) at middepth in the via on the sidewall.

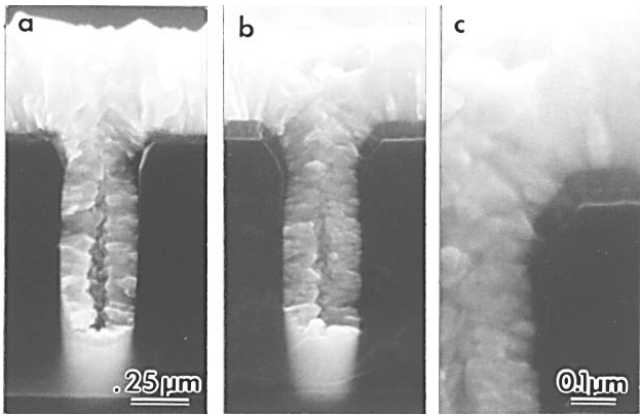

Figure 11. SEM micrograph of oxide via filled with WCVD/TiN/250 Å Ti, with a plasma preclean (set III): (a) 50 Å TiN, (b) 500 Å TiN, and (c) detail with 500 Å TiN.

Both the Ti and TiN films were measured to have ~5% of the surface thickness on the sidewalls, although the bottom of the via had approximately 40% of the surface film thickness. No obvious difference in step coverage in the via is observed with different tungsten CVD gas ratios during nucleation. The plasma preclean had an obvious beneficial influence for step coverage due to the improved TiN/Ti profile at the top corner of the via (Fig. 10). The sidewall of the via is now tapered 1700 Å down into the via prior to TiN/Ti deposition (Fig. 11). Thicker TiN films can be used in vias that have been plasma precleaned without sacrificing step coverage. For this study, adequate step coverage was achieved with 30:30 tungsten gas flow nucleation films, allowing for the use of thin TiN barriers. For vias with higher aspect ratios, this may not be the case (*i.e.*, step coverage may not be adequate for 30:30 flow ratios).

Conclusion

Several parameters that influence the volcano reaction in oxide vias between tungsten CVD and sputter deposited TiN/Ti films have been investigated. Higher WF_6:SiH_4 ratios during deposition of tungsten nucleation films increased fluorine penetration and the likelihood of volcanoes. Thin TiN barriers also increased volcano occurrence, but rapid thermal annealing prior to tungsten CVD or a plasma preclean prior to TiN/Ti deposition can allow the use of thin TiN without volcanoes. The plasma preclean has a greater effect than the RTA, allowing only 50 Å of IMP TiN (without an RTA) to protect Ti, as opposed to 100 Å TiN with an RTA (without a plasma preclean).

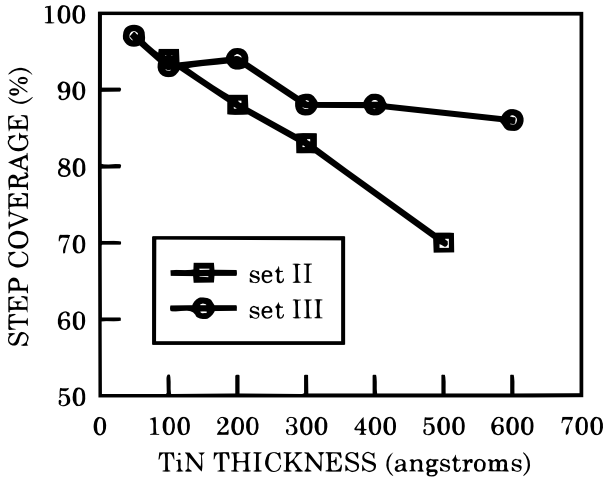

Figure 10. Plot of step coverage with TiN thickness for various process conditions.

Without either of these treatments, 400 Å of IMP TiN was needed to prevent volcano formation. Besides fluorine penetration, stress plays a role in the volcano formation, as evidenced by the plasma preclean effect and depositions of tungsten CVD at lower temperatures. The mechanism by which stress affects volcano occurrence requires further modeling and study to fully understand. Overall step coverage of tungsten CVD films was found to increase almost linearly with decreasing TiN film thickness, due to the profile of the barrier film at the surface edge of the via, and was further improved with a plasma preclean prior to TiN/Ti deposition. Though we have investigated four of the parameters affecting volcano reaction, many remain to be investigated: the influence of the titanium film thickness and profile, the partial pressures of WF_6 and SiH_4 for same gas ratios, the H_2 and Ar gas flows during nucleation, tungsten nucleation film thickness, and via shape (*e.g.*, parallel *vs.* bevel-shaped sidewalls).

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EXHIBIT D

Silicon VLSI Technology

Fundamentals, Practice and Modeling

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hin Film Deposition

9

Introduction

The CMOS process flow in Chapter 2 contained many layers above the silicon substrate. These layers include dielectrics, semiconductors, and metals. In most cases these layers must be deposited which implies that there are typically many deposition steps in an IC process. In this chapter we describe the different techniques used to deposit these thin films. In Chapter 10 the techniques used to etch thin films are discussed.

We begin with several issues related to thin films and their deposition. These issues are important when evaluating deposited films and choosing deposition methods. The first issue is the "quality" of the deposited film. By quality we mean composition, contamination levels, defect density, and mechanical and electrical properties. The composition of films may vary depending on the deposition conditions and it is usually important to achieve a specific composition. This is especially important when a range of compositions is possible, such as with TiN films which can be Ti or N rich, or with alloys of metals like Al/Cu. Generally there needs to be a low level of contaminants, such as unwanted metals, water, oxygen, or halogens. There should also be a minimum of pin holes or other structural defects. These often result from particle contamination on the surface and are a common problem in thin film deposition (recall Figure 4–1). There should also be a minimum of stress in the films, and the films should be mechanically stable during subsequent processing. Finally, good adhesion to underlying films is important.

A second issue is that of uniform thickness across a wafer, from wafer to wafer, and as the film crosses nonplanar topography. Figure 9–1 shows a metal layer deposited over nonplanar topography in which there is a step in the underlying oxide. In Figure 9–1(b) the film thickness decreases as it crosses a step, which can lead to high electrical resistance in metal lines and a greater chance of mechanical cracking and failure. Coverage on the side of a step in topography is called step coverage. It is often defined quantitatively as the minimum thickness deposited on the side of a step divided by the thickness deposited on the top horizontal surface. Conformal step coverage, or conformal coverage, refers to uniform film thickness on both horizontal and vertical surfaces, or a step coverage of one.

A related issue is that of filling spaces between or within topographical structures. This includes filling a via or contact hole with metal, as illustrated in Figure 9–2(a), and filling spaces or gaps in shallow trench isolation structures or between metal lines with an oxide (often called gap filling), as illustrated in Figure 9–2(b). In this figure incomplete filling is shown, leading to a void in the dielectric between the lines. A void in a metal layer can lead to high-contact or -sheet resistance, and in a dielectric layer can

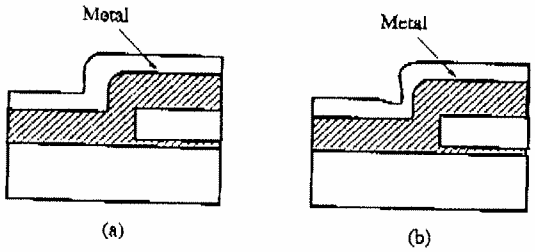

Figure 9–1 Step coverage of metal over nonplanar topography. (a) shows conformal step coverage, with constant thickness on horizontal and vertical surfaces. (b) shows poor step coverage.

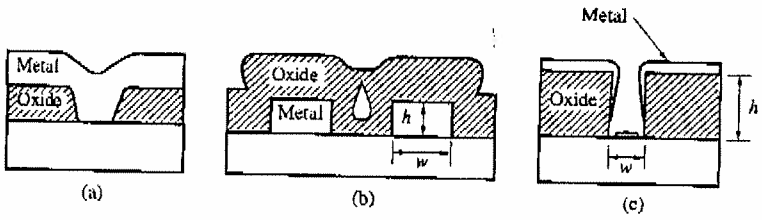

Figure 9–2 Thin film filling issues. (a) shows good metal filling of a via or contact hole in a dielectric layer. (b) shows silicon dioxide dielectric filling the space between metal lines, with poor filling leading to void formation. (c) shows poor filling of the bottom of a via hole with a barrier or contact metal.

result in cracking problems. In addition, a void may trap processing chemicals or moisture, leading to reliability problems. Even if complete filling of a space is not needed, good coverage or filling at the bottom of a space is often required. An example of this is the case of depositing contact and barrier layers, in which good filling of the bottom of contact or via holes is important. Figure 9–2(c) shows poor bottom coverage of a deep contact hole. The sides may also need adequate coverage of an adhesion layer.

An important parameter that can affect filling and bottom coverage is the Aspect Ratio (AR) of a feature, defined as the ratio of the height of a feature to its width:

$$AR = \frac{\text{height of feature}}{\text{width of feature}} = \frac{h}{w} \tag{9.1}$$

The feature could be a metal line, for example, or a space, such as a gap between two metal lines or a contact hole, as illustrated in Figure 9–2(b) and (c). A deep, narrow contact hole would have a large aspect ratio and would be harder to fill.

Two examples of poor filling and coverage are shown in Figure 9–3. Figure 9–3(a) shows poor step coverage of a TiW/Al/TiW metal stack layer over an oxide step. Figure 9–3(b) shows voids in an oxide layer for narrow spaces between metal lines. We will see that in filling or depositing in very deep contacts or vias, conditions that would lead to good step coverage may actually hinder adequate filling of the bottom of the contacts or vias.

We saw in the CMOS process flow in Chapter 2 that as more interconnect levels are used, another property that is desired for thin films is a smooth and flat top surface, as op-

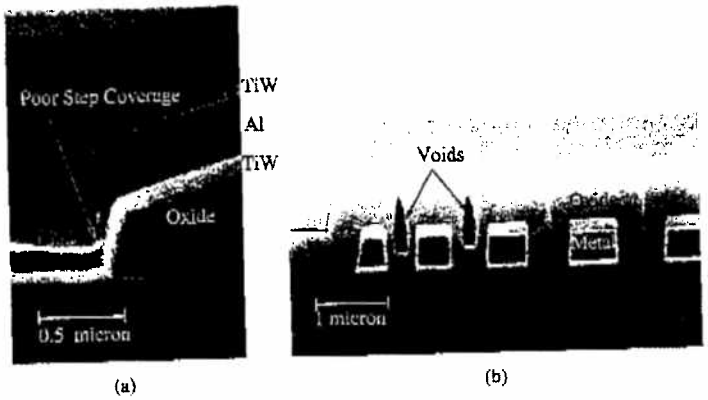

Figure 9–3 SEM images of coverage and filling problems. (a) shows poor step coverage of a TiW/Al/TiW metal stack layer, deposited by sputter deposition, over an oxide step. (b) shows voids in a Chemical Vapor Deposition (CVD) oxide layer for narrow spaces between metal lines. Photos courtesy of VLSI Technology, Inc.

posed to one that just follows the underlying topography. Figure 9–3(b) shows a relatively flat, planarized top surface of the oxide over the metal lines. While planarized topography can be achieved by postdeposition processing using etching or polishing techniques, we will also see how certain deposition techniques can also help attain this feature.

9.2 Historical Development and Basic Concepts

Methods of thin film deposition are usually separated into two main categories: Chemical Vapor Deposition (CVD) and Physical Vapor Deposition (PVD). In each case the silicon wafer is placed in a deposition chamber, and the constituents of the film are delivered through the gas phase to the surface of the substrate where they form the film. In the case of CVD, reactant gases are introduced into the deposition chamber, and chemical reactions between the reactant gases on the substrate surface are used to produce the film. In the case of PVD, physical methods are used to produce the constituent atoms which pass through a low-pressure gas phase and then condense on the substrate. The methods used to produce the atom flux in PVD include (1) heating a solid or molten source until it vaporizes, called "evaporation," and (2) bombarding a solid source with energetic ions formed in a plasma, called "sputter deposition." PVD is sometimes called "vacuum deposition" since very low-pressure environments are required for the transport of the gaseous species from the source to the film surface. (As we will see, low-pressure CVD is commonly used, but not at nearly as low pressures as in PVD.) CVD has historically been used in the integrated circuit industry mainly for silicon and dielectric deposition, primarily due to its good quality films and good step coverage. PVD has been used historically for metal deposition, mostly due to its ability to deposit a variety of metals and alloys not easily deposited by CVD.

A third category for thin film deposition is the technique of coating a wafer with a liquid film that forms a solid film when heated. Spin-On-Glasses (SOGs) are examples of this. This method, which is used for topography smoothing or "planarization," will be discussed in Chapter 11. A fourth category includes electrolytic deposition techniques. These have historically been used for printed circuit board fabrication but have recently been extended to the deposition of Cu interconnect layers.

9.2.1 Chemical Vapor Deposition (CVD)

In CVD, gases are introduced into the deposition chamber that react and form the desired film on the surface of the substrate. The silicon substrate will usually have other films deposited and patterned on it which then form a complex topography on which the new film must be deposited. Either a single gas is used that will decompose when heated to supply the necessary component or components for the film, or multiple gases are used which will react to produce the film. In either case, the film-producing reaction should take place on the surface of the substrate as opposed to in the gas stream. Gas stream reactions can create particulates that form above the wafer which can drop down onto the surface and cause the films to have pinholes or low density. Sometimes appropriate reactants are not available in gaseous form, in which case a liquid source may be used. A carrier gas such as hydrogen is bubbled through the liquid source and carries the source vapor to the reaction chamber. Nitrogen or argon may be used as a diluent or carrier gas.

The simplest CVD process uses an atmospheric deposition chamber, and no plasma-enhanced processes are used. This is appropriately called Atmospheric Pressure Chemical Vapor Deposition, or APCVD. The configuration shown in Figure 9–4(a) is a common type that has been used for APCVD, especially for epitaxial silicon deposition, but several other systems in a variety of configurations such as barrel-shaped chambers, have been used. The walls of the chamber in this case are not heated—a so-called "cold-wall" reactor. The wafers are heated by using a graphite susceptor which is heated by RF induction. This minimizes deposition on the reactor walls since only the susceptor and wafers are hot. APCVD has been used for many films, especially epitaxial silicon and silicon dioxide—both undoped and doped with boron and phosphorus. However, the increasing use of Low-Pressure CVD, or LPCVD, and Plasma-Enhanced CVD, or PECVD, for reasons to be discussed in the following sections, has made the use of APCVD reactors much less common today.

Figure 9–4(b) shows the low-pressure CVD configuration. In this case the wafers are stacked upright, and the deposition is performed at a reduced pressure. Heating is accomplished using resistive heating elements wrapped around the tube (a "hot-wall" reactor), which heats up the tube and everything inside. This is very similar to the oxidation system described in Chapter 6. Very uniform temperatures can be obtained in this type of system.

There are other types of CVD configurations and techniques, but all are based on the idea of supplying gaseous chemical sources and energy to the surface of the wafers. The energy is usually thermal energy, but one can greatly reduce the amount of thermal energy needed by using a plasma to provide for energetic ions and very reactive free radicals to stimulate the deposition.

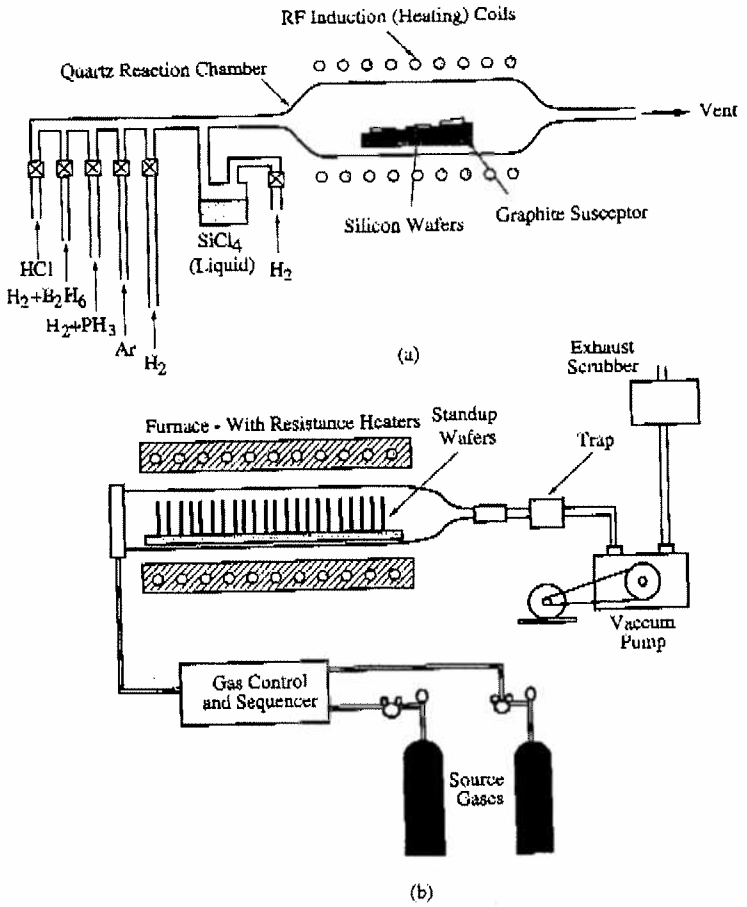

Figure 9–4 Chemical Vapor Deposition (CVD) systems. (a) is an atmospheric cold-wall system used for deposition of epitaxial silicon. (b) is a low-pressure hot-wall system used for deposition of polycrystalline and amorphous films, such as polysilicon and silicon dioxide, respectively.

9.2.1.1 Atmospheric Pressure Chemical Vapor Deposition (APCVD)

Although APCVD systems are not used as commonly today, we will begin with an APCVD system to describe some of the basic concepts of CVD. The steps involved in a CVD process, schematically illustrated in Figure 9–5, are

1. Transport of reactants by forced convection to the deposition region.
2. Transport of reactants by diffusion from the main gas stream through the boundary layer to the wafer surface.

EXHIBIT E

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Enhanced Metalorganic Chemical Vapor Deposition Titanium Nitride Film Fabricated Using Tetrakis-Dimethylamino-Titanium for Barrier Metal Application in Sub-Half-Micron Technology

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Enhanced metalorganic chemical vapor deposition (MOCVD) titanium nitride (TiN:C) film with low resistivity ($< 700\,\mu\Omega \cdot$ cm) has been fabricated by thermal decomposition of tetrakis-dimethylamino-titanium (TDMAT; $Ti[N(CH_3)_2]_4$). Enhancement is carried out by *in-situ* N_2 plasma treatment of as-deposited TiN:C film and the enhanced TiN:C film has good stability: less than 4% increase in film resistivity after exposure to air for 24 days. The amount of oxygen absorbed in this enhanced TiN:C film after air exposure, determined by Auger electron spectroscopy (AES) was significantly reduced. This enhanced MOCVD TiN:C film has been successfully applied to sub-half-micron devices. A void-tree tungsten plug (W plug) for sub-half-micron holes can be achieved. Good barrier performance and low contact/via resistance have also been demonstrated.

KEYWORDS: MOCVD, TiN:C, TDMAT, N_2 plasma, W plug

1. Introduction

For ultralarge-scale integrated (ULSI) circuits, titanium nitride (TiN) film deposited by physical vapor deposition (PVD) has been widely used as the barrier layer in aluminum and tungsten metallization processes.[1–5] However, as the feature size of devices continuously decreases to 0.35 μm and below, the significant increase in aspect ratio for smaller contact and via holes adversely affects the barrier performance of PVD TiN film, due to its poor step coverage. The overhang phenomenon at the top corner of holes also decreases the remaining aperture, thus affecting subsequent metallization steps. These issues limit the extension of the PVD TiN process to deep sub-half-micron technology.

Therefore, a significant amount of work has been carried out with the aim of developing a chemical vapor deposition (CVD) TiN process.[6–13] There are several chemistries which can be used for CVD TiN deposition. In one approach, $TiCl_4$ reacts with either NH_3 or N_2. However, this chemistry usually results in the incorporation of chlorine (Cl) in the film unless the processing temperature is very high enough that will eventually prevent its application in metal via. The presence of Cl always causes concerns regarding corrosion-related reliability issues and seriously restricts the application of this CVD TiN process in multilevel interconnect technology. An alternative is the use of metalorganic chemistries to deposit TiN film below 400°C. Other approaches for depositing conformal TiN films using metalorganic chemistry and ammonia have been reported.[6–8] Recent investigations on TiN film deposited using TDMAT revealed that thermal decomposition of TDMAT results in carbon-rich films with high resistivity.[9–11] Oxygen absorbed into the as-deposited TiN:C film after air exposure further increases the film resistivity.[14] The high degree of oxygen absorption and high resistivity of MOCVD TiN:C films formed by thermal decomposition of TDMAT are the major problems which prevent this process from being applied to multilevel interconnects.

In this work, we report that the application of *in-situ* N_2 plasma treatment to as-deposited TiN:C films formed by thermal decomposition of TDMAT effectively reduces the film resistivity and enhances the film stability, while maintaining excellent step coverage. Such enhanced TiN:C films were successfully applied to sub-half-micron technology. Good barrier and low contact/via resistances were obtained.

2. Experimental

The MOCVD TiN:C films were deposited in a CVD chamber (Applied Materials) which could be used for *in-situ* N_2 plasma treatment. A schematic diagram of the chamber is shown in Fig. 1. Thermal decomposition of TDMAT on a hot wafer surface results in the deposition of TiN:C film. Helium (He) is used to carry TDMAT into the process chamber. A summary of the process conditions is given in Table I. The chamber pressure and susceptor temperature are 300 mTorr and 420°C, respectively. Due to the temperature offset of 60–70°C between the wafer and susceptor, the actual process temperature of the wafer is around 350–360°C. RF power applied to the bottom electrode is the source which generates the

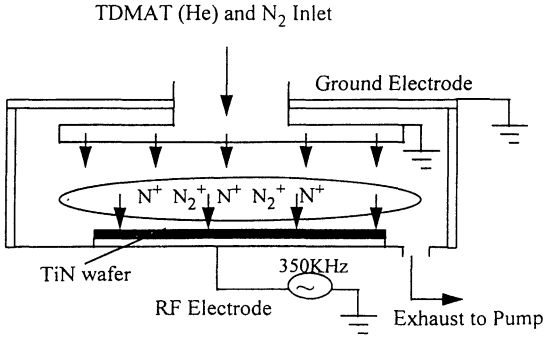

Fig. 1. Schematic diagram of process chamber used for enhanced MOCVD TiN:C film deposition.

Table I. Summary of process conditions for MOCVD TiN:C film deposition.

Temperature (°C)	420
Pressure (mTorr)	450
Spacing (mm)	11.5
He flow rate (sccm)	400

Table II. Process conditions for N_2 plasma treatment for enhancement of MOCVD TiN:C films.

Temperature (°C)	420
Pressure (mTorr)	300
Spacing (mm)	19
Power (W)	200
N_2 flow rate (sccm)	200

N_2 plasma. *In-situ* N_2 plasma treatment is performed immediately after the deposition of TiN:C film. The process conditions used for N_2 plasma treatment are shown in Table II.

The step coverage of as-deposited MOCVD TiN:C on sub-half-micron holes was investigated by scanning electron microscopy (SEM). The film resistivity was measured using a four-point probe. Auger electron spectroscopy (AES) and Rutherford backscattering (RBS) were used to determine the absorbed oxygen content and the composition of the TiN:C films. Cross-sectional transmission electron microscopy (XTEM) was used to investigate W plug integration.

The enhanced MOCVD TiN:C films were integrated with a tungsten plug (W plug) metallization process at both the contact and via levels to evaluate their electrical characteristics.

3. Results and Discussion

3.1 *Characterization of enhanced MOCVD TiN:C films*

Figure 2 shows a SEM micrograph of the step coverage of an enhanced MOCVD TiN:C film. Compared to PVD TiN films, this enhanced MOCVD TiN:C film has very good conformality; the step coverage exceeds 70% for 0.3 μm holes with an aspect ratio of more than 3. As reported by Eizenberg *et al.*[15] this good conformality is due to the fact that MOCVD TiN:C is deposited under conditions in which the surface reaction is controlled in the temperature range of 275–360°C.

Figure 3 shows the resistivity of MOCVD TiN:C film as a function of air exposure time. For MOCVD TiN:C films without N_2 plasma treatment, the resistivity is quite high ($> 1 \times 10^4\ \mu\Omega \cdot$ cm) and extremely variable. However, the resistivity of MOCVD TiN:C films after *in-situ* N_2 plasma treatment is around 700 $\mu\Omega \cdot$ cm and is almost independent of air exposure time. In terms of resistivity, the relatively good stability of this enhanced MOCVD TiN:C film is shown in Fig. 4 (less than 4% increase in film resistivity after exposure to air for 24 days). Figure 5 shows the oxygen content in the MOCVD TiN:C films due to air exposure determined by AES. For MOCVD TiN:C films without N_2 plasma treatment, there is a rapid increase in oxygen concentration with time. The concentration is as high as 19 at.% after exposure to air for 24 days. An AES depth profile of oxygen in an as-deposited TiN:C film after expo-

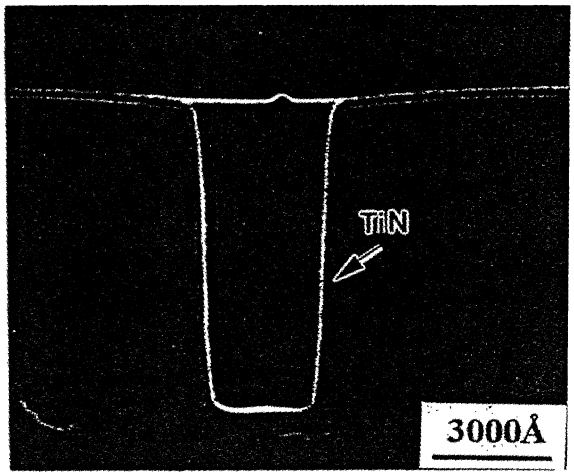

Fig. 2. SEM micrograph showing the excellent step coverage of MOCVD TiN:C film.

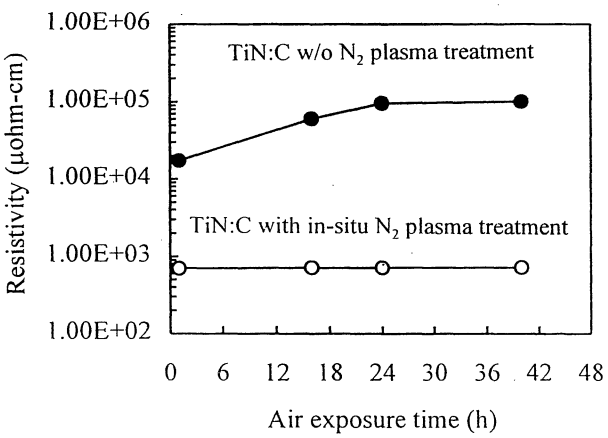

Fig. 3. The dependence of resistivities of as-deposited MOCVD TiN:C and enhanced TiN:C on air exposure time. The thickness of the films is 200 Å.

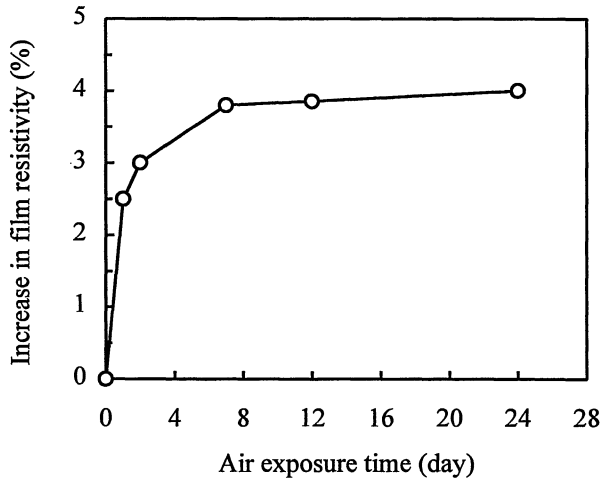

Fig. 4. The relationship between the resistivity increase of enhanced MOCVD TiN:C film and air exposure time. The thickness of the films is 200 Å.

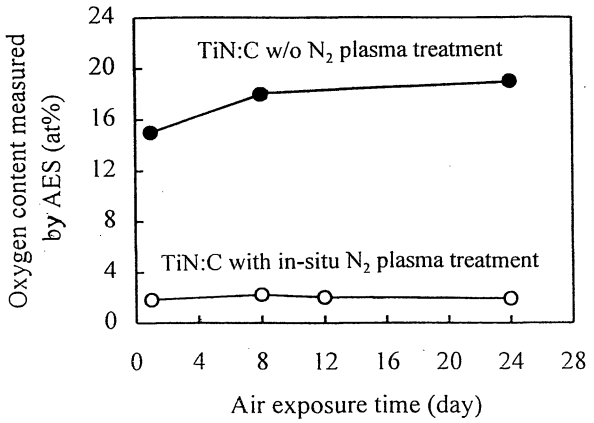

Fig. 5. The oxygen content in as-deposited MOCVD TiN:C and enhanced TiN:C films due to air exposure (determined by AES analysis). The thickness of the films is 200 Å.

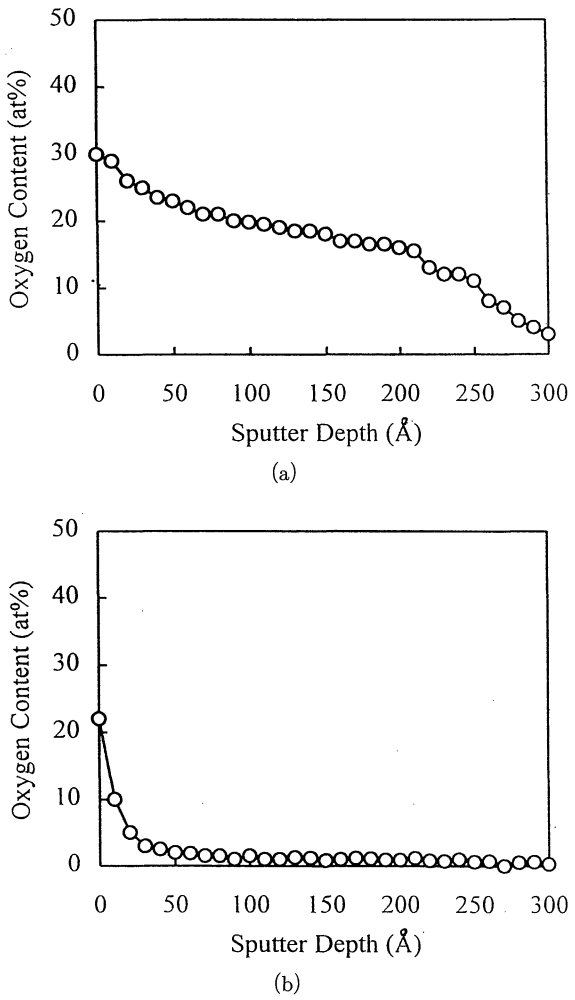

Fig. 6. (a) Depth profile of oxygen in as-deposited MOCVD TiN:C film after air exposure for 8 h determined by AES analysis. The thickness of the films is 200 Å. (b) Depth profile of oxygen in enhanced MOCVD TiN:C film after air exposure for 8 h determined by AES analysis. The thickness of the films is 200 Å.

sure to air for 8 h is shown in Fig. 6(a). Apparently, the oxygen absorption is due to the diffusion of oxygen species from the surface into the bulk. The as-deposited MOCVD TiN:C film is assumed to be porous in order to explain the high and unstable resistivity as well as the high level of oxygen absorption in MOCVD TiN:C films without N_2 plasma treatment. *In-situ* N_2 plasma treatment of as-deposited TiN:C films can effectively after the porous microstructure by the incorporation of nitrogen (N) species, which enhance the film stability and reduce the resistivity. Thus, the absorbed oxygen content can be limited to less than 3 at.%. The corresponding AES results are shown in Figs. 5 and 6(b). As the RBS analysis results in Table III show, the MOCVD TiN:C film with *in-situ* N_2 plasma treatment has a N-rich composition and lower carbon and oxygen content than that of an as-deposited TiN:C film. The effect of N_2 plasma treatment has carried

out after air exposure is quite limited. Once a TiN:C film has absorbed a large amount of oxygen and obtained a high resistivity, an incident N_2 plasma cannot replace oxygen in the film and reduce the resistivity. Therefore, to achieve film enhancement, *in-situ* N_2 plasma treatment is essential.

Table III. Compositions of as-deposited MOCVD TiN:C and enhanced MOCVD TiN:C films measured by RBS.

	C (at.%)	N (at.%)	O (at.%)	Ti (at.%)	N/Ti ratio
as-deposited CVD TiN:C	30	23	20	27	0.85
enhanced CVD TiN:C	23	44	3	30	1.47

The efficiency of N_2 plasma treatment in resistivity reduction was evaluated as a function of deposited TiN:C film thickness. Figure 7 shows the increase in resistivity reduction as the TiN:C thickness decreases. The rate of increase decreases after the deposition thickness decreases below 100 Å. To achieve film resistivity as low as 600 $\mu\Omega \cdot$ cm, N_2 plasma treatment of 50 Å MOCVD TiN:C film is necessary. However, if both wafer throughput and film resistivity are considered, N_2 plasma treatment of 100 Å MOCVD TiN:C films is appropriate to achieve film resistivity of 800 $\mu\Omega \cdot$ cm. Therefore, to obtain 200 Å enhanced TiN:C film, 2 cycles of 100 Å film deposition followed by *in-situ* N_2 plasma treatment are required.

3.2 *Process integration of enhanced TiN:C with W plug*

The enhanced MOCVD TiN:C films were applied to sub-half-micron devices as diffusion barriers and adhesive layers for W plug application. Prior to the deposition of enhanced TiN:C film, a titanium (Ti) underlayer was deposited. After deposition of the enhanced TiN:C film, blanket tungsten deposition and tungsten etchback to form W plug were carried out. Then, aluminum-copper alloy was deposited and patterned to construct interconnects. As the XTEM micrograph of the via structure in Fig. 8 shows, void-free W plugs for sub-half-micron holes can be fabricated easily due to the excellent conformality of the MOCVD TiN:C process. The uniform thickness of the TiN:C barrier layer presents on the bottom and bottom corner of holes, which provides sufficient barrier

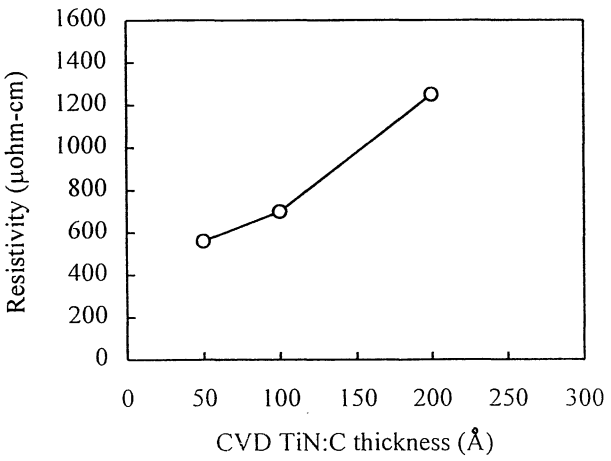

Fig. 7. The relationship between the efficiency of N_2 plasma treatment in resistivity reduction and the thickness of the deposited TiN:C film.

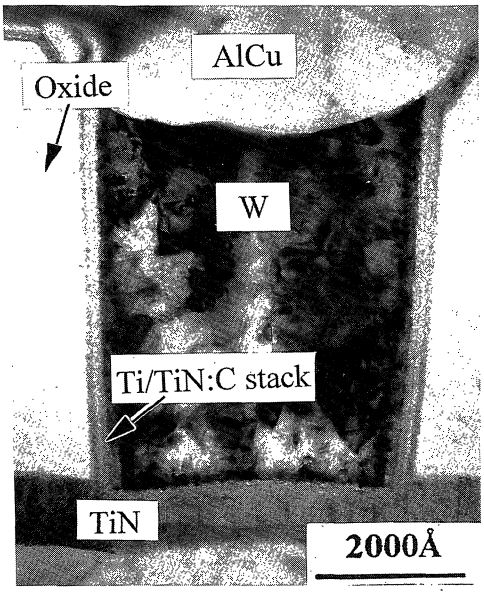

Fig. 8. Cross-sectional TEM micrograph showing void-free W plug metallization with enhanced MOCVD TiN:C as the underlayer.

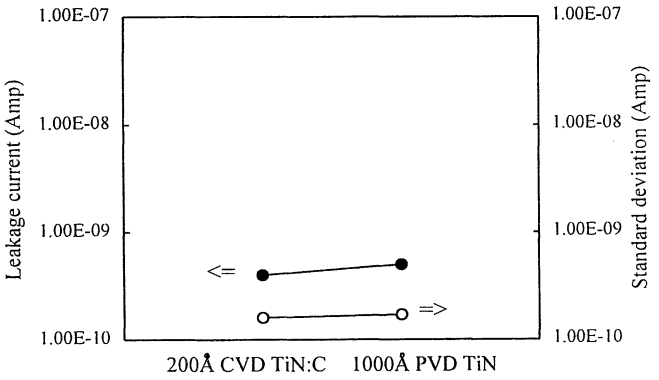

Fig. 9. Leakage current performance of N+/P diode with either PVD TiN or enhanced MOCVD TiN:C as the barrier layer.

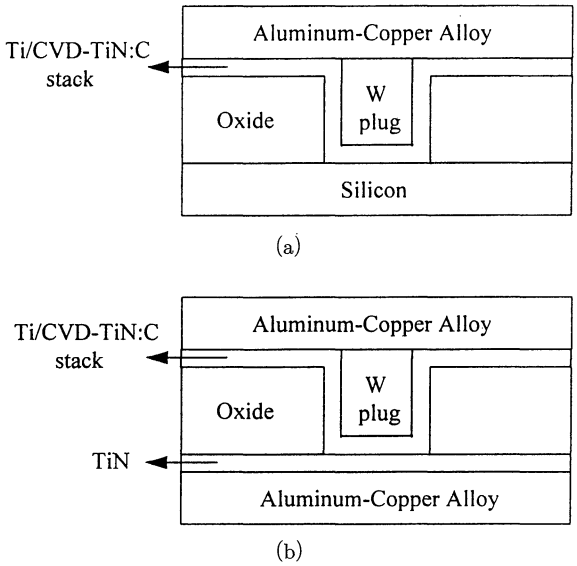

Fig. 10. (a) Schematic cross-sectional view of contact structure. (b) Schematic cross-sectional view of via structure.

properties. Not only is the volcano phenomenon due to the reaction of penetrating WF_6 and the Ti underlayer during W deposition easily prevented but also consistently low junction leakage is achieved, as described below.

In order to verify the electrical characteristics of the enhanced TiN:C film, an enhanced TiN:C film 200 Å thick formed by two cycles of *in-situ* N_2 plasma treatment and a PVD TiN film 1000 Å thick are chosen in order to obtain the same bottom thickness inside contact and via holes. The results of the PVD TiN process are used as a reference. Figure 9 shows the leakage current performance of a N+/P contact for the enhanced MOCVD TiN:C barrier system. In terms of leakage current, the enhanced TiN:C film 200 Å thick is slightly better than the PVD TiN film 1000 Å thick. The standard deviation of the leakage current is also lower. This is directly related to the better bottom step coverage and barrier properties of enhanced TiN:C film. A chain structure of contacts and vias with sizes ranging from 0.35 μm to 0.60 μm fabricated over silicon in the case of contacts and over aluminum-copper alloy/TiN underlayers in the case of vias was used to evaluate contact/via resistances. Schematic cross-sectional views of the contact and via structures are shown in Figs. 10(a) and 10(b), respectively. In order to make good ohmic contact with silicon, a Ti layer 400 Å thick was deposited prior to deposition of the TiN barrier. The contact resistances of both the enhanced TiN:C and the PVD TiN are shown in Fig. 11. Due to the reduced contact area, the contact resistance increases as the contact size decreases. Moreover, the two curves for 200 Å enhanced TiN:C and 1000 Å PVD TiN almost overlap each other. This indicates that contact resistance in these two cases is similar. Because the crucial factors which determine the contact resistance on silicon are a clean interface, efficient dopant activation and sufficient thickness of Ti deposited at the contact bottom, the contribution due to the resistance of TiN film can be neglected. This

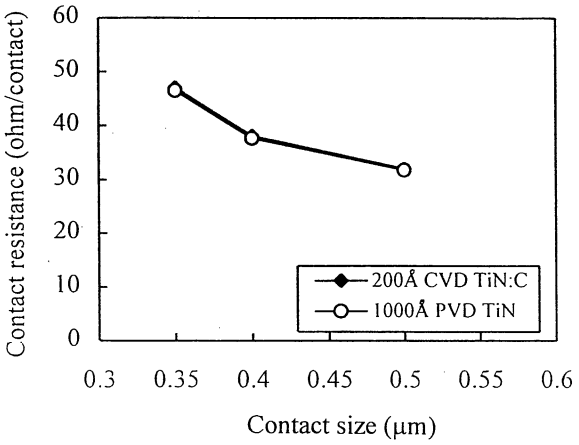

Fig. 11. Contact resistances (R_{c_N+}) by using PVD TiN and enhanced MOCVD TiN:C barrier layers for various contact sizes.

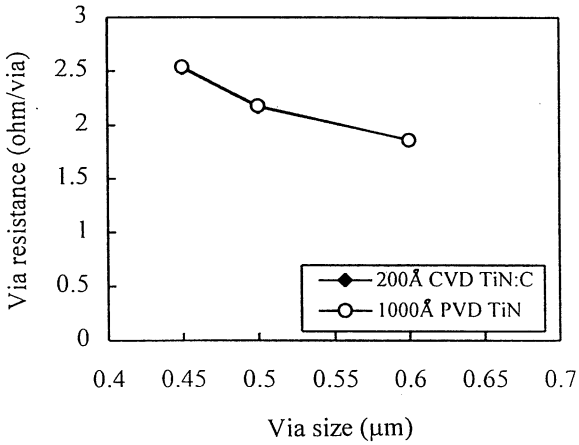

Fig. 12. Via resistance (R_{c_via}) by using PVD TiN and enhanced MOCVD TiN:C barrier layers for various via sizes.

explains the comparable contact resistances on silicon of enhanced TiN:C and PVD TiN. The contact resistances of via holes (R_{c_via}) are shown in Fig. 12. Similar to the comparison on contact resistance, for depositing either 200 Å enhanced TiN:C film or 1000 Å PVD TiN film, the values of R_{c_via} are very similar and the curves overlap each other. In both cases, the values of R_{c_via} increase from 1.8 Ω/via to around 2.5 Ω/via as the via size decreases from 0.6 μm to 0.45 μm. Since the contact resistance of via holes (R_{c_via}) is quite low ($< 3\,\Omega$/via) and the resistivity of the enhanced TiN:C films is high ($> 500\,\mu\Omega\cdot$cm), the contribution of the TiN:C film resistance to R_{c_via} was taken into account and evaluated as a function of MOCVD TiN:C film thickness. As shown in Fig. 13, R_{c_via} increases with the deposited TiN:C thickness. This is probably due to the fact that a higher R_{c_via} corresponds to a greater TiN:C film thickness at the bottom of the via hole.

4. Conclusions

An enhanced MOCVD TiN:C film formed by thermal decomposition of TDMAT has been developed and has low, stable resistivity. Enhancement by *in-situ* N_2 plasma treatment of the as-deposited MOCVD TiN:C

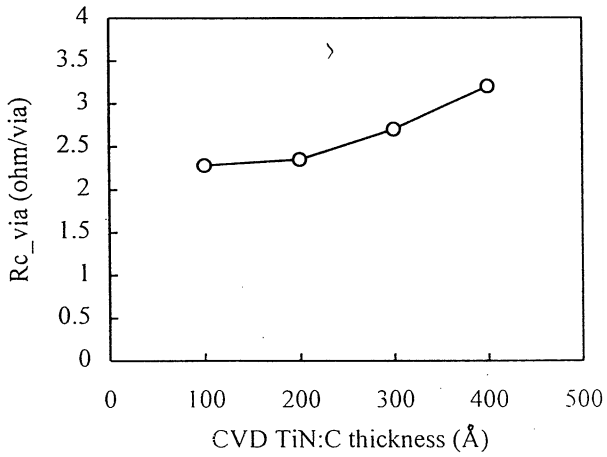

Fig. 13. The relationship between via resistance (R_{c_via}) and the thickness of enhanced MOCVD TiN:C film. The via size is 0.45 μm.

film is the key to reducing the film resistivity and stabilizing the film properties by incorporation of nitrogen species. Enhanced TiN:C film has been successfully applied to W plug metallization for sub-half-micron contact and via holes. The conformal characteristic of enhanced MOCVD TiN:C film results in excellent barrier performance and thus easier process integration. Acceptable low values of contact and via resistances can also be obtained.

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EXHIBIT F

SILICON PROCESSING FOR THE VLSI ERA

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PROCESS TECHNOLOGY

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Chapter 6

CHEMICAL VAPOR DEPOSITION of AMORPHOUS and POLYCRYSTALLINE THIN FILMS

Chemical vapor deposition (CVD) is defined as the formation of a solid film on a substrate by the reaction of vapor-phase chemicals (reactants) that contain the required constituents. The reactant gases are introduced into a reaction chamber and are decomposed and/or reacted at a heated surface to form the thin film. Note that in CVD the reactant gases do not react with (and therefore do not consume) any substrate surface material. A wide variety of thin films utilized in ULSI fabrication are formed by CVD.[1,2] The deposition of amorphous and polycrystalline thin films by CVD is the subject of this chapter. The growth of single-crystal silicon films by CVD epitaxial techniques is described in Chap. 7.

The fundamental principles of CVD involve a wide variety of scientific and technical disciplines, including gas-phase reaction chemistry, thermodynamics, kinetics, heat transfer, fluid mechanics, surface reactions, plasma reactions, film growth phenomena, and reactor engineering. Obviously these interdisciplinary principles can only be covered very briefly here. Interested readers should consult references for more information on these topics.[3,4]

In this chapter, the mechanisms and a model for thin film growth in CVD are discussed first. Next, the deposition technology and equipment used to prepare such films by CVD are covered. Finally, we consider the properties and deposition conditions of some of the most widely used films deposited by CVD (including polycrystalline silicon, silicon dioxide, silicon nitride, tungsten, aluminum, tungsten silicide, and titanium nitride). Also note that the measurement of many of the properties of CVD films is virtually identical to the measurement of the same properties in other thin films. Thus, only the measurement of those properties that are unique to the specific thin films under discussion will be mentioned here. Readers should consult the index for information on various generic thin film measurement methods.

As discussed in Chap. 4, thin films are used in a host of different applications in ULSI fabrication, and can be prepared using a variety of techniques. Regardless of the method by which they are formed, however, the process must be economical, and the resultant films must exhibit the following characteristics: a) good thickness uniformity; b) high purity and density; c) controlled composition and stoichiometry; d) high degree of structural perfection; e) good electrical properties; f) excellent adhesion; g) good step coverage; and h) low defect density.

Specific deposition methods have been developed to fabricate such thin films, based on the required capabilities for satisfying these demanding criteria. CVD processes are often selected over competing deposition techniques because they offer the following advantages: a) high purity deposits can be achieved; b) a great variety of chemical compositions can be deposited; c) some films cannot be deposited with adequate film properties by any other method; and d) good economy and process control are possible for many CVD deposited films.

6.1 BASIC ASPECTS OF CHEMICAL VAPOR DEPOSITION

A CVD process can be summarized as consisting of the following sequence of steps:

1. A given composition of reactant gases (frequently diluted by mixing with an inert *carrier* or *diluent* gas) is introduced by forced convection into a reaction chamber. These gases move in the chamber from the inlet to the outlet in what is referred to as the *main gas-flow region*, as shown in Fig. 6-1a). As these gases flow through the chamber, they come into the vicinity of the wafers that have been loaded within it.

2. The reactant-gas species are transported to the wafer surface through a sector of the gaseous volume referred to as the *boundary layer*. This transport occurs by gas-phase diffusion. That is, a boundary layer in the gas exists between the main gas-flow region and surface of the wafer (Figs. 6-1a and b).

3. The reactants are adsorbed on the substrate surface, and these adsorbed species are referred to as *adatoms*.

4. The adatoms undergo surface migration to the growth sites, where the *film-forming chemical reactions* take place. These reactions are responsible for creating the solid film and gaseous by-products. In some cases, a gas-phase reaction leading to the formation of film precursors (or even the final product) occurs somewhere in the gas prior to the reactants reaching the substrate surface.

5. The gaseous by-products of the reaction are desorbed from the surface. These products must diffuse through the boundary layer near the surface into the main gas-flow region, and from there they are removed from the chamber as the main gas-flow moves toward the outlet.

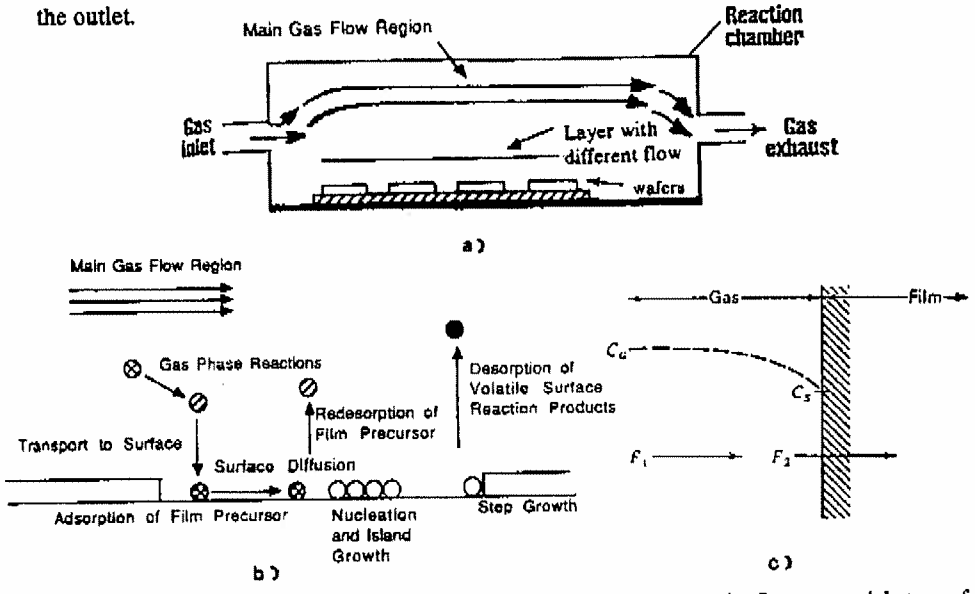

Fig. 6-1 a) CVD reaction chamber with gases flowing into and out of it. b) The five sequential steps of a CVD process. c) Grove's model of the CVD process depicting the transport and reaction fluxes F_1 and F_2.

Energy to drive the film forming reactions is supplied by one or more of the following energy sources: thermal energy; photons; or electrons (with thermal energy being the most common energy source used). A variety of chemical reaction types are employed in CVD to fabricate the many kinds of films needed in ULSI structures, including pyrolysis (thermal decomposition), reduction, oxidation, disproportionation, and hydrolysis of the reactants.

Several other practical aspects of CVD processes should be mentioned. First, the deposition time needed to form the film with the desired thickness must be sufficiently short to permit adequate wafer throughput. Second, the process temperature must be low enough so that it does not adversely impact the stability of previously deposited layers (e.g., low-melting-point metal layers such as Al). Third, the CVD process should not allow by-products of the reactant gases to become incorporated into the growing films (but this is sometimes unavoidable, such as when a significant amount of hydrogen is incorporated in PECVD silicon nitride films - see Sect. 6.5).

As noted in Step 4, the chemical reactions leading to the formation of the solid that makes up the deposited film may, in practice, take place not only on (or very close to) the wafer surface (*heterogeneous reaction*), but also in the gas phase (*homogeneous reaction*). Heterogeneous reactions are preferred, as such reactions occur selectively only on heated surfaces, and produce good quality films. Homogeneous reactions are undesirable because they form solid clusters of the depositing material in the gas phase. These clusters can rain down on the film growing on the wafers, which may cause defects in the depositing film and other film problems including poor adhesion and low film density. In addition, homogeneous reactions also consume reactants and thus can cause the deposition rate to decrease. As a result, one important characteristic of a chemical reaction for CVD application is the degree to which heterogeneous reactions are favored over gas-phase reactions.

6.1.1 Grove's Simplified CVD Film-Growth Model

Since the aforementioned steps of a CVD process are sequential, the one which occurs at the slowest rate will determine the overall rate of the film deposition. This slowest step is referred to as the *growth-rate-limiting step*. Since high growth rates are essential for making a deposition process economically feasible, the determination of the growth-rate-limiting step can be valuable. Knowledge of which of the five steps is the slowest may allow process modifications to be developed to speed up that step, and perhaps increase the overall deposition rate.

A model that allows the growth rate of CVD films to be predicted would also be a useful tool for developing CVD processes. However, deriving a mathematical relationship which predicts CVD growth rates based on all five steps of the process sequence has proven difficult, even up to this time. Instead, less complex growth-rate models have been created, based on the observation that the steps of the CVD process can be grouped into two categories: 1) those that occur in the gas phase (*gas-phase processes*); and 2) those that occur on the substrate surface or chamber-wall surface (*surface processes*). For example, by using this observation, Grove[5] developed a simple CVD growth-rate model in 1966 that is still widely used. Grove's model assumes that *only one of the gas-phase growth steps* (i.e., the transport of the reactants across the boundary layer, Step 2 *or only one of the surface processes* (i.e., the surface chemical reaction, Step 4) *is the rate-limiting step*. Despite these simplifying assumptions, Grove's model explains many phenomena observed in CVD processes and predicts many film growth rates quite accurately.

Chapter 11

ALUMINUM THIN FILMS and PHYSICAL VAPOR DEPOSITION in ULSI

This chapter is divided into three major topics involved in the formation of interconnect structures in VLSI. These topics are:

1. *The Properties of Aluminum (and Aluminum Alloy) Thin Films in ULSI.* This section considers the advantages and limitations of Al and Al-alloy thin films for ULSI applications. It should be noted that many of the fabrication processes that involve aluminum are also discussed elsewhere in the chapter (e.g., the deposition of aluminum films by sputtering), or in other chapters of this volume (e.g., dry etching of aluminum in Chap. 14). Several issues associated with the use of thin film aluminum are addressed in other parts of this text as well, including: a) step coverage; b) effects of gas incorporation in the deposited film; c) electromigration (Vol. 2 of this series); d) hillocks in Al thin films and their suppression (Vol. 2); and e) contact formation to silicon, including spiking, contact electromigration failure, and contact structures/barrier layers (here and Vol. 2).

2. *Physical Vapor Deposition (PVD) by Sputtering.* The discussion on sputtering is quite extensive, as this is the primary PVD method utilized in ULSI applications. The sputtering presentation covers the following subjects: a) glow-discharge physics; b) the physics of sputtering; c) deposition kinetics of sputtered films; d) sputter system configurations (dc, rf, and magnetron); e) commercially available sputtering equipment for microelectronic applications; and f) sputter deposition processing issues.

3. *Thickness Evaluation of Opaque (Especially Metallic) Thin Films.*

Since the key topic of this chapter is *physical vapor deposition* (PVD), it is useful to define the concept and introduce the common characteristics shared by PVD processes. All PVD processes proceed according to the following sequence of steps:

1. The material to be deposited (from a solid or liquid source) is physically converted to the vapor phase.
2. The vapor is transported across a region of reduced pressure (from the source to the substrate).
3. If the substrate is located near the surface being vaporized, some of the vapor produced can condense to form a thin solid film on the substrate.

In sputter deposition, the conversion to a gaseous phase (Step 1) is done by the physical dislodgment of surface atoms by momentum transfer. This step will receive the most attention in the chapter, because some aspects of film condensation and formation were discussed in earlier chapters dealing with thin films, epitaxy, and CVD. It should also be noted that many concepts

Table 11-1 PROPERTIES OF ALUMINUM AND ALUMINUM ALLOY THIN FILMS

Name	Symbol	Melting Point (°C)	Al/Si Eutectic (°C)	Density (g/cm^3)	Resistivity ($\mu\Omega$-cm)
Aluminum	Al	660	577	2.70	2.7
Aluminum/ 4% Copper	Al 4%Cu	650	~577	2.95	3.0
Aluminum/ 2% Silicon	Al 2%Si	640	~577	2.69	2.9
Aluminum/ 4% Copper 2% Silicon	Al 4%Cu 2%Si		~577	2.93	3.2

used to describe PVD processes, including vacuum pressure, mean free path, impingement rate, monolayer time, vapor pressure, and gas flow regimes were presented in Chap. 3.

11.1 ALUMINUM THIN FILMS IN ULSI

Aluminum has historically been the third material in the trinity of matrix substances employed to fabricate Si-based solid-state components (the other two being Si and SiO_2). Aluminum and Al-alloy thin films were selected as the workhorse materials for interconnect structures for the first 30 years of the IC industry. As of 1999 Al-alloys continue to be the most widely used materials for IC metallizations, although copper films are beginning to emerge as probable replacements. The dominance of Al for interconnect applications arose because of its low resistivity (ρ_{Al} = 2.7 $\mu\Omega$-cm), and its compatibility with the other two matrix substances.[1,2] Aluminum thin films adhere well to SiO_2, because (during the thermal step that sinters the Al-Si contacts) some of the Al atop the SiO_2 reduces some of the SiO_2 layer to form a thin layer of Al_2O_3 at the Al/SiO_2 interface. This promotes good adhesion between SiO_2 and Al.

Table 11-1 lists the material properties of Al thin films of most interest for silicon device fabrication. The table also indicates that Al alloys are utilized in microelectronic applications, and in fact, films of such alloys are used instead of pure-Al films. The Al alloys that have found most use include: a) Al:1wt%Si; b) Al:2wt%Cu; c) Al:1wt%Si:2wt%Cu; and d) Al:1.2%Si:0.15wt%Ti. Each will be discussed below. Note that the relatively low values of the melting point of Al (660°C) and the Al-Si eutectic temperature (577°C) restrict the value of subsequent processing temperatures once Al films have been deposited.

Thin films of sputtered aluminum are typically deposited in the thickness range of 500–1500 nm, and these films have a polycrystalline structure. Early microelectronic devices utilized evaporation to deposit pure Al and Al:Si or Al:Cu alloys. However, the stringent alloy-composition requirements of advanced devices (as well as some other limitations of evaporation) gave sputtering an advantage over evaporation for depositing metal films. The development of magnetron sputtering (which allows aluminum to be deposited at deposition rates of up to ~1000 nm/min), caused sputtering to entirely displace evaporation as the PVD technology for depositing Al-alloy films in VLSI and ULSI fabrication. Aluminum alloy films also replaced pure Al films because the alloys possess enhanced properties for certain interconnect requirements, including superior contact formation characteristics and better resistance to electromigration. A brief introduction to these topics follows (see also Vol. 2 of this series).

The use of *Al:Si* in place of *pure Al* stems from the problem of *junction spiking* that occurs at the interface of pure Al and Si. That is, the solubility of silicon in aluminum (Fig. 11-1) rises as the temperature increases (e.g., to about 0.5% at 400°C). When a Si substrate is put into intimate contact with a pure Al film, the wafer becomes a source of Si that can dissolve in the solid Al solvent. In addition, the diffusivity of silicon along the grain-boundaries of the alum-inum film at 400°C is quite high. Thus, a significant quantity of Si can move from the region beneath the Al/Si-substrate interface into the aluminum film. Simultaneously, Al from the film will move to fill the voids created by the departing Si (Fig. 11-2). If the aluminum penetrates deeper than the *pn* junction depth beneath the contact, the junction will be electrically shorted (junction spiking). One way to suppress this set of events is to use an alloy of Al with a con-centration of Si that exceeds the solubility limit of Si at the maximum process temperature, *in lieu* of pure Al. In that case, when the (Al:Si alloy)/Si interface is heated the Al:Si alloy film cannot dissolve additional silicon originating from the substrate, and junction spiking is avoided.

Although this remedy was once effective, it became inadequate for ULSI applications. The shallower junctions and narrow metal lines are less tolerant of the Si precipitation occurring in these Al alloy films as they cool down from the 400°C steps. The Al-alloy films become super-saturated with Si as they cool down, causingitto precipitate. In addition, electromigration failure of the Al:Si-silicon contacts becomes more severe as the contacts get smaller. Thus, the use of Al-Si alloy films to combat junction spiking in ULSI devices was abandoned in favor of contact structures employing barrier layers. The most widely used barrier layer in ULSI is titanium nitride (TiN). Discussion of the deposition of such TiN layers by PVD is given in a later section, and by CVD in Chap. 8. More information on contacts between interconnect materials and the Si substrate is also found in Chap. 15. (See also Vol. 2 of this series for a detailed discussion of the topic of metal-silicon contacts and the inadequacies of Al:Si for VLSI and ULSI).

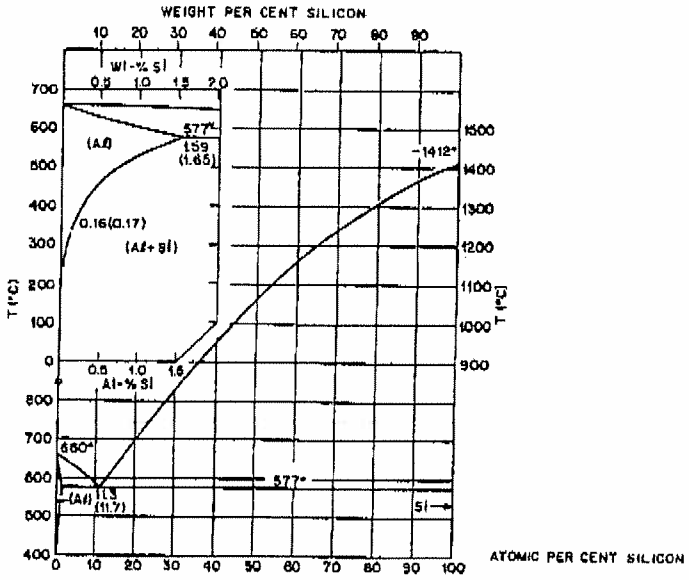

Fig. 11-1 Phase diagram of the aluminum-silicon system. From M. Hansen and A. Anderko, *Constitution of Binary Alloys*, 1958. Reprinted with permission of McGraw-Hill Book Co.[3]

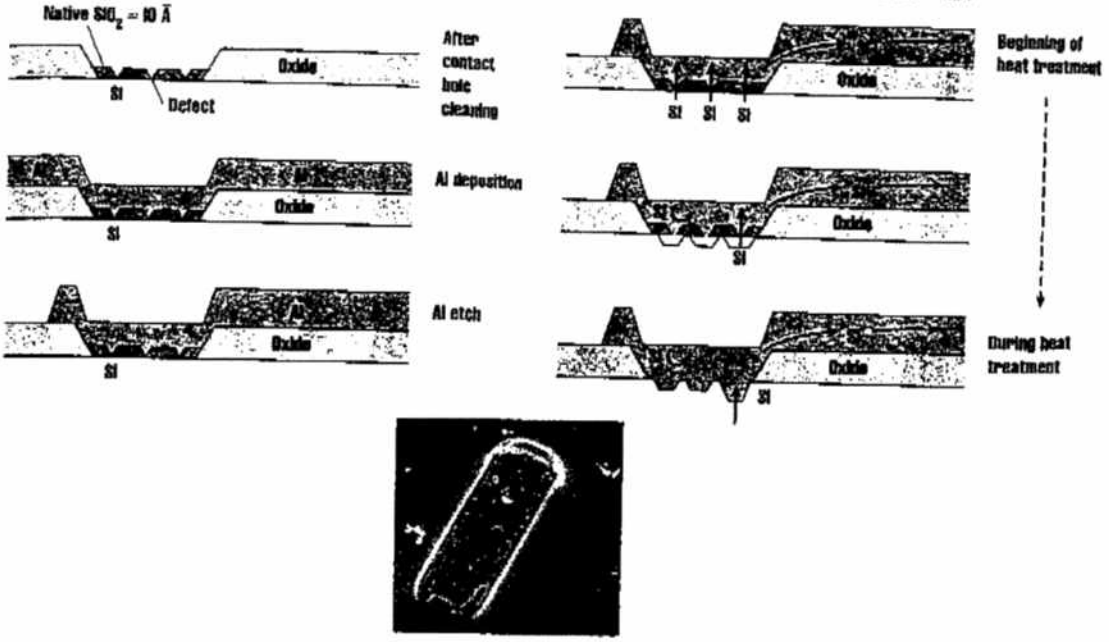

Fig. 11-2 Junction spiking and silicon migration during contact sintering.

It has also been found that the addition of small quantities (0.1–4%) of other materials (e.g., Cu [0.5–4wt%] and Ti [0.1–0.5wt%]) to the aluminum improves the electromigration resistance and reduces the propensity of aluminum thin-films to form hillocks (i.e., protrusions on the Al film surface). One penalty for enhancing these characteristics of Al films is that their resistivity is increased (by 10–30%) over that of pure aluminum films (see Table 11-1). Other drawbacks that must be accepted to gain the improvements offered by Al alloys include added process complexity, and more stringent process controls. An appropriate combination of alloy composition, film deposition, annealing, and etch processes must be selected, developed, evaluated, and maintained. Furthermore, some processes are more difficult to perform on alloy films than on pure Al films, such as dry etching of Al:Cu films (Chap. 14). Details of the issues that must be considered in developing and evaluating processes that utilize Al alloy films are discussed elsewhere, both in this text and in Vol. 2.

Some other characteristics of Al thin films need to be presented at this point. Aluminum readily forms a thin native oxide (Al_2O_3) on its surface upon exposure to oxygen, even at room temperature. The presence of this oxide can affect the contact resistance when another metal layer is deposited onto the Al, and can inhibit both the sputtering of an aluminum target and the etching of aluminum films. Aluminum thin films can also suffer corrosion problems as a result of some fabrication processes. For example, if phosphorus-doped SiO_2 is deposited onto Al films, phosphoric acid (HPO_3) can be formed if moisture is absorbed by the glass. This acid will attack Al and cause corrosion. In addition, dry etching of Al may leave chlorine residues on the Al surfaces. Exposure of these residues to ambient moisture can lead to the formation of HCl. If Cu is present as an alloy in the Al film, severe corrosion can occur (as the $CuAl_2$ compound and the Al form the microelectrodes of a battery, and HCl acts as the electrolyte). Both of these problems are discussed elsewhere in the text in more detail (see Index, under *Al, corrosion*).

11.2 SPUTTER DEPOSITION FOR ULSI

Sputtering is a term used to describe the mechanism in which atoms are ejected from the surface of a material when that surface is struck by sufficiently energetic particles. It has become the dominant technique for depositing a variety of metallic films in VLSI and ULSI fabrication, including aluminum alloys, titanium, titanium:tungsten, titanium nitride, tantalum, and cobalt.

Sputtering displaced the original PVD technique for depositing metal films (evaporation) for the following reasons:

1. Sputtering can be accomplished from large-area targets, which simplifies the problem of depositing films with uniform thickness over large wafers.
2. Film thickness control is relatively easily achieved by selecting a constant set of operating conditions, and then adjusting the deposition time to reach it.
3. The alloy composition of sputter-deposited films can be more tightly (and easily) controlled than that of evaporated films.
4. Many important film properties, such as step coverage and grain structure can be controlled by varying the negative bias and heat applied to the wafers. Other film properties (including stress and adhesion), can be controlled by altering such process parameters as power & pressure.
5. The surface of the substrates can be sputter-cleaned in vacuum prior to initiating film deposition (and the surface is not exposed again to ambient after such cleaning).
6. There is sufficient material in most sputter targets to allow many deposition runs before target replacement is necessary.
7. Device damage from x-rays generated during electron-beam evaporation is eliminated (although some other radiation damage may still occur).

As is true with other processes, however, sputtering also has its drawbacks. They include:

1. Sputtering processes involve high capital equipment costs;
2. Since the process is carried out in low-medium vacuum ranges (compared to the high vacuum conditions under which evaporation is conducted), there is greater possibility of incorporating impurities into the deposited film.
3. Better step coverage can generally be achieved using CVD.

In general, the sputtering process consists of four steps:

1. Ions are generated and directed at a target.
2. The ions sputter target atoms;
3. The ejected (sputtered) atoms are transported to the substrate.
4. Upon reaching the substrate they condense and form a thin film.

Although it is of interest to note that sputtering can be conducted by generating the energetic incident ions by other means (e.g., ion beams), in virtually all VLSI and ULSI sputtering processes their source is a glow-discharge. The discussion of sputtering in this section will be limited to *glow-discharge sputtering*.[4,5,6]

11.2.1 Introduction to Glow Discharge Physics

The energetic particles used to strike target materials to be sputtered in ULSI sputter deposition systems are generated by glow-discharges.[4,5] A *glow-discharge* is a self-sustaining type of plasma (a *plasma* is defined as a partially ionized gas containing an equal number of positive and negative charges as well as some number of neutral gas particles). In Fig. 11-3 a simple *dc-diode type* system that can be employed to study properties of glow discharges used in

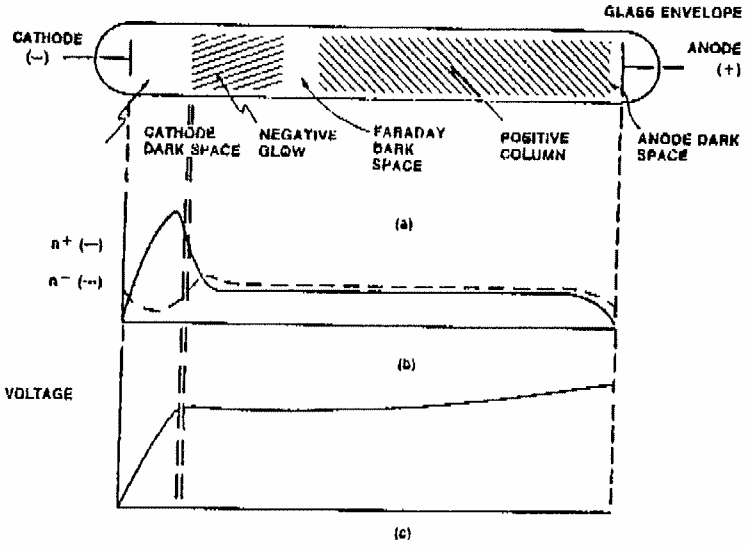

Fig. 11-3 (a) Structure of a glow discharge in a dc diode system. (b) Charged particle concentration in a glow discharge. (c) Voltage variation in a dc diode glow discharge.

sputtering is shown. It consists of a glass tube that is evacuated and then re-filled with a gas at low pressure. Within the tube there are two electrodes (a positively charged *anode* and a negatively charged *cathode*) and a dc potential difference is applied between them.

11.2.2 The Creation of Glow Discharges

Consider the system shown in Fig. 11-3 to examine the case when a tube is filled with Ar at an initial pressure of 1 torr, the distance between the electrodes is 15 cm, and a 1.5 kV potential difference is applied between them. At the outset no current flows in the circuit, as all the Ar gas atoms are neutral and there are no charged particles in the gas. The full 1.5 kV is thus dropped between the two electrodes. If a free electron enters the tube (most likely created from the ionization of an Ar atom by a passing cosmic ray), it will be accelerated by the electric field existing between the electrodes (whose magnitude is: $E = V/d = 1.5\ kV/15\ cm = 100\ V/cm$).

The average distance that a free electron will travel at $P = 1$ torr before colliding with an Ar atom (i.e., the mean free path λ) is 0.0122 cm (Chap. 3). Most electron-atom collisions are *elastic*, in which virtually no energy is transferred between the electron and gas atom. Such elastic collisions occur because the mass of the electron is much smaller than that of the atom. Thus, the minumum distance an electron must travel before it can undergo an *inelastic* collision (in which significant energy *is* transferred to the atom, either by the excitation of an atomic electron to a higher energy level, or to cause its escape from the atom) is about ten times λ, or 0.122 cm. If this is the minimum distance that must be traveled by electrons between inelastic collisions, there must be a significant number of electron path lengths in the range of 0.5–1.0 cm. If a free electron travels 1 cm in the 100 V/cm electric field, it will have picked up 100 eV of kinetic energy. With this amount of energy, the free electron can transfer enough energy to an Ar electron to cause it to be excited or ionized. If this transferred energy E is less than the ionization potential (e.g., $11.5\ eV < E < 15.7\ eV$ for Ar), the orbital electron will be excited to a

EXHIBIT G

NP

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,607	06/13/2001	Vincent Fortin	M-11469 US	6406

7590 04/23/2002

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No.	Applicant(s)	
	09/881,607	FORTIN, VINCENT	
	Examiner	Art Unit	
	Long K. Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14,21,22,26 and 27 is/are rejected.

7)☐ Claim(s) 15-20 and 23-25 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: Page 5, line 3; change "110.2" to -- 110 --.

Appropriate correction is required.

Election/Restrictions

2. Applicant's election of claims **1 - 27** in Paper No. **5** is acknowledged.

3. This application contains claims **28 - 34** drawn to an invention non-elected in Paper No. **5**. A complete reply to the final rejection must include cancellation of non-elected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Information Disclosure Statement

4. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statements (IDS) were considered.

Information disclosure papers have been filed.

Claim Rejections - 35 USC § 112

5. Claims 26-27 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: claims 1 and 21 are method and claims 26-27 are apparatus. The apparatus claims could not depend from method claims. Claims 26-27 are required amendment or cancellation.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims **1 – 5, 9, 12** and **26** are rejected under 35 U.S.C. 102(b) as being anticipated by Fiordalice et al. (US Patent No. 5,420,072).

Regarding claims **1, 12** and **26**, Fiordalice et al. disclose a fabrication method comprising:

forming a titanium nitride layer 22/24 (fig. 3) over a substrate (fig. 1; col. 2, lines 21-47) by physical vapor deposition, the titanium nitride layer being less than 30 nm thick (col. 2, line 61-63);

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound (col. 2, lines 56+; col. 3, lines 1+); and then

forming a tungsten layer 26 (fig. 3; col. 4, line 37-39) over and in physical contact with the titanium nitride layer 24 (fig. 3) by chemical vapor deposition (col. 2, lines 56+; col. 3, lines 1+).

Regarding claim **2**, Fiordalice et al. disclose a titanium nitride layer is formed by Sputtering (col. 1, lines11-13).

Regarding claims **3, 4** and **5**, Fiordalice et al. disclose a titanium nitride layer is less than 25 nm thick; less than 22 nm thick; and about 20 nm thick (col. 2, lines61-63; col. 3, lines 41-43).

Regarding claim **9**, Fiordalice et al. disclose the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature above 600°C (col. 2, lines 54+; col. 3, lines 1-3).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **10,11**are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiordalice et al. (US Patent No. 5,420,072)

Regarding to claims **10** and **11**, Fiordalice et al. disclose step of exposing the titanium nitride layer to the nitrogen an/or the nitrogen compound at a temperature range from 300°C to 800°C (col. 3, line 2-3) except for the amount of time is 20 – 40 seconds.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to expose the titanium nitride layer to the nitrogen an/or the nitrogen compound for about 20-40 seconds, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

10. Claims **6- 8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fiordalice et al. (US Patent No. 5,420,072) in view of Yamamori (US Patent No. 5,731,225).

Regarding claims **6 - 8**, Fiordalice et al. disclose the claimed invention except for forming a titanium layer before the titanium nitride layer, the titanium nitride layer being in physical contact with the titanium layer; the titanium is less than 36nm thick; and the titanium is about 10nm thick

Yamamori discloses method of forming Ti layer 14 (fig. 1B) before forming TiN layer 15 (fig. 1B) to prevent voids in the plugs because tungsten tens to attack Ti; the Ti layer is formed by sputtering up to a thickness of 10nm to 100nm.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to add a step of adding titanium before the titanium nitride layer as disclosed by Yamamori into Fiordalice 's method in order to decrease contact resistances with the silicon substrate and the polysilicon layer, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin V. Erlichman, 168 USPG 177, 179*

11. Claims **13, 21,22 and 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fiordalice et al. (US Patent No. 5,420,072) in view of Nagamine et al. (US Patent No. 6,287,988).

Regarding claims **13, 21, 22 and 27**, Fiordalice et al. disclose method of forming a circuit element in or over the substrate; forming an insulating layer over the substrate and the circuit element (col. 2, line 21+);

forming a titanium nitride layer being less than 25 nm thick (col. 2, line 61-63), the titanium nitride layer being formed by sputtering (col. 1, lines11-13);

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound (col. 2, lines 56+; col. 3, lines 1+);

forming an opening 16 (fig. 2) in the insulating layer, the opening exposing the circuit element 20 (fig. 2);

wherein the titanium nitride layer and the tungsten layer 30 (fig. 6; col. 4, lines 59-62) are present in the opening and the tungsten layer at least partially filling the opening and electrically contacts the circuit element through the titanium nitride layer 24 (fig.6) in the opening.

Fiordalice et al. do not explicitly disclose a trench is at least 2 μm long.

Nagamine et al. disclose a trench with a depth of 4 μm (col. 38, line 67; col. 39, line 1) Nagamine et al. also disclose a trench with a depth of .4 μm (col. 38, line 58-59) as an element isolation trench.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to apply a 4 μm trench per Nagamine design for Fiordalice device in order to meet their specific application as the applicant's invention, since such a modification would have involved a mere change in the size of a component. A

change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

In addition Fiordalice et al. do not disclose forming a titanium layer over the insulating layer, the titanium layer overlaying sidewalls of the opening, the titanium layer being less than 15 nm thick; and forming a titanium nitride layer over the titanium layer. See the previous respond to claims 6-8 above.

Allowable Subject Matter

12. Claims 14 - 20 and 23 -25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to teach a trench with at least 1 mm long.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran

April 18, 2002

HOAI HO
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/881,607	Applicant(s)/Patent Under Reexamination FORTIN, VINCENT	
	Examiner Long K. Tran	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,420,072	05-1995	Fiordalice et al.	427/126.1
	B	US-5,731,225	03-1998	Yamamori, Atsushi	438/653
	C	US-6,287,988	09-2001	Nagamine et al.	438/765
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EXHIBIT H

#74
7/30/02
amr

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Fortin, Vincent		
Assignee:	Mosel Vitelic, Inc.		
Title:	Thin Titanium Nitride Layers Used In Conjunction With Tungsten		
Serial No.:	09/881,607	Filing Date:	June 13, 2001
Examiner:	Tran, Long K.	Group Art Unit:	2818
Docket No.:	M-11469 US		

San Jose, California
July 17, 2002

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

AMENDMENT

Sir:

Responsive to the Office Action mailed 23 April 2002, please amend the above patent application as follows:

IN THE SPECIFICATION

Page 2, amend the paragraph beginning on line 11 to read

--The inventor has determined that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers. In some embodiments, fewer volcanoes have been observed with a TiN layer thickness of 20 nm than with 30 nm. In fact, no volcanoes have been observed in some structures formed with the 20 nm TiN layers. Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers and a higher density of the TiN grains.--

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Page 3, amend the paragraph beginning at line 18 to read

--The photoresist was removed, and another layer of photoresist (not shown) was deposited and patterned photolithographically to define a trench 470 in dielectric 110 for a tungsten interconnect. The length of the trench 470 was normally at least 2μm. In some embodiments, the trench length was approximately 1 mm. The trench width was then 0.22 μm. The trench was etched with a timed etch to a depth of approximately 250 nm. Via 464 was fully exposed at the bottom of the trench.--

Page 4, amend the paragraph beginning at line 6 to read

--The thickness of Ti layer 140 was varied. In one embodiment, the thickness was less than 36 nm, preferably less than 15 nm, more preferably less than 12 nm, typically 10 nm. In another embodiment, the thickness was 36 nm.--

Page 4, amend the paragraph beginning at line 15 to read

--In one embodiment, the thickness of TiN layer 150 was less than 30 nm, preferably less than 25 nm, more preferably less than 22 nm, typically 20 nm. The thickness of the TiN layer 150 was 30 nm in another embodiment.--

Page 4, amend the paragraph beginning at line 17 to read

--Then the structure was heated to a temperature between 600°C and 700°C for 20 to 40 seconds, typically 20 to 30 seconds, in a nitrogen atmosphere. (This operation is referred to herein as Rapid Thermal Anneal, or RTA.) The base pressure was 100-120 torr, the nitrogen flow was 8 slm (standard liters per minute). The temperature was 620°C in one embodiment, 670°C in another embodiment. The anneal was performed in a system of type HEATPULSE 8800 available from AG Associates, Inc., of San Jose, California. The anneal is believed to have increased the lateral size of TiN grains 150G (Fig. 3).--

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Page 5, amend the paragraph beginning at line 3 to read

A5

--Then the layers 160, 150, 140 were polished off the top of dielectric 110 by CMP. The resulting structure is shown in Fig. 6. Prior to CMP, the structure was examined for volcanoes using an optical microscope and SEM and STEM microscopes. The results are given in Table 1 below. The second column of Table 1 indicates the temperature of the Rapid Thermal Anneal, described above, performed after the deposition of TiN 150 before the deposition of tungsten 160. In Embodiment No. 1, the anneal was omitted.--

Page 5, amend the paragraph beginning at line 12 to read

A6

--These results show, unexpectedly, that the use of thinner Ti and TiN layers in combination with the RTA can provide a better protection against the volcanoes than thicker layers without the RTA. The thinner layers can eliminate the volcanoes at the lower RTA temperature of 620°C. Lower RTA temperatures are desirable to reduce impurity diffusion during the RTA, to prevent melting or softening of materials having low melting temperatures (e.g. aluminum), and reduce wafer warping. In any event, the sputter deposited TiN layers, such as TiN layer 150, have substantially a columnar grain structure.--

Enclosed are copies of specification pages 2 - 5 in which the changes to the foregoing paragraphs are indicated in red.

IN THE CLAIMS

Page 7, line 1, change "CLAIMS" TO --I CLAIM:--.

Amend Claims 6, 9, 13, 15, 18, 24, and 25 to read:

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A7 5--6. (Amended) The method of Claim 1 further comprising forming a titanium layer before forming the titanium nitride layer, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

A8 8 9. (Amended) The method of Claim 1 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600°C.

A9 11 18 12 17. (Amended) The method of Claim 12 further comprising:

forming a circuit element in or over the substrate;

forming an insulating layer over the substrate and the circuit element;

forming an opening in the insulating layer, the opening exposing the circuit element, the opening comprising a trench at least 2 μm long;

wherein the titanium nitride layer and the tungsten layer extend into the opening, and the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening.

A10 13 16. (Amended) The method of Claim 12 13 further comprising depositing a titanium layer over the insulating layer before forming the titanium nitride layer, wherein the tungsten layer electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening.

A11 15 18. (Amended) The method of Claim 12 13 wherein the circuit element comprises metal or semiconductor material.

A12 28 24. (Amended) The method of Claim 21 25 wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 670°C for 20-40 seconds.

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29 25. (Amended) The method of Claim 21 wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a temperature of about 620°C for 20 - 40 seconds.--

A 12 Cont

Enclosed is an appendix which indicates how the above version of Claims 6, 9, 13, 15, 18, 24, and 25 is produced from the previous version of those claims. In the appendix, added material is underlined, and deleted material is in brackets.

Cancel Claims 28 - 34 without prejudice.

Add new Claims 35 - 37 as follows:

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30 25
35. The method of Claim 21 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least 600°C.

20 19
36. The structure of Claim 26 wherein the titanium nitride layer has a substantially columnar grain structure.

22 21
37. The structure of Claim 21 wherein the titanium nitride layer has a substantially columnar grain structure.

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REMARKS

Several changes have been made in the specification to correct a self-evident error, to clarify how the inventor developed the invention, and to conform the specification with other parts of the application as filed. More particularly, the invention's Summary on page 2 has been modified to provide that "The inventor has determined", rather than "discovered", "that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers". Per the Examiner's request, the reference-symbol error that occurs near the top of page 5 has been corrected.

Originally filed Claims 6, 21, and 34 respectively provide that the titanium layer is less than 36 nm thick, less than 15 nm thick, and less than 12 nm thick. On page 4 of the specification, the sentence providing that the thickness of Ti layer 140 was 10 nm has been modified to provide that the thickness of this Ti layer "was less than 36 nm, preferably less than 15 nm, more preferably less than 12 nm, typically 10 nm", thereby conforming the specification to the originally filed claims with respect to the thickness of the titanium layer.

Originally filed Claims 1, 3, and 4 respectively provide that the titanium nitride layer is less than 30 nm thick, less than 25 nm thick, and less than 22 nm thick. On page 4 of the specification, the sentence providing that the thickness of TiN layer 150 was 20 nm in one embodiment and 30 nm in another embodiment has been divided into two sentences. One of the sentences provides that "In one embodiment, the thickness of TiN layer 150 was less than 30 nm, preferably less than 25 nm, more preferably less than 22 nm, typically 20 nm". The other sentence provides that "The thickness of the TiN layer 150 was 30 nm in another embodiment". These revisions conform the specification to the originally filed claims with respect to the thickness of the titanium nitride layer.

Originally filed Claims 10, 11, 24, and 25 all provide that the heating step is performed for 20 - 40 seconds. On page 4 of the specification, the sentence providing that the structure was heated to a temperature of 600 - 700°C for 20 to 30 seconds in a nitrogen atmosphere has been modified to provide that "Then the structure was heated to a temperature between 600°C and 700°C for 20 to 40 seconds, typically 20 to 30 seconds, in a nitrogen

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atmosphere." This modification conforms the specification to the originally filed claims with respect to the duration of the heating step.

Originally filed Claim 28 provides that the titanium nitride layer has a "substantially columnar grain structure". On page 5 of the specification, a sentence has been added at the end of the paragraph that follows Table 1 and deals with the advantages of the invention to state that "the sputter deposited TiN layers, such as TiN layer 150, have substantially a columnar grain structure". This revision conforms the specification to the originally filed with respect to the nature of the grain structure of titanium nitride layers formed according to the invention.

Turning to the claims, dependent Claims 6, 9, 13, 15, 18, 24, and 25 have been amended to improve the grammar and clarify the nature of the invention. Claims 28 - 34 have been canceled in light of the Restriction Requirement. Dependent Claims 35 - 37 have been added to claim the invention with more particularity. Accordingly, Claims 1 - 27 and 35 - 37 are now pending.

With respect to the amendment of dependent Claim 9 which previously recited "a temperature above 600°C", lines 17 and 18 of the specification recite that "the structure was heated to a temperature between 600°C and 700°C". This reasonably means that the temperature was at least 600°C and up to 700°C. Accordingly, Claim 9 has been revised to recite that the temperature during the heating step is "at least" 600°C. New dependent Claim 35 adds the same limitation for the chain of claims beginning with Claim 21.

Claims 26 and 27 have been rejected under 35 USC 112 as "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections". With apparent reference to the fact that Claims 26 and 27 are structure claims which respectively depend from method Claims 1 and 21, the Examiner alleges that "The apparatus claims could not depend from method claims". This rejection is respectfully traversed.

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Claims 26 and 27 are product-by-process claims. As stated in the Manual of Patent Examining Procedure, section 2173.05(p), August 2001, page 2100-205, copy enclosed,

> A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper. . . . A claim to a device, apparatus, manufacture, or composition of matter may contain a reference to the process in which it is intended to be used without being objectionable under 35 U.S.C. 112, second paragraph, so long as it is clear that the claim is directed to the product and not the process.

Furthermore the fact that Claims 26 and 27 are dependent claims does not make them improper. As earlier stated in the Manual of Patent Examining Procedure, section 608.01(n), August 2001, page 600-77, copy enclosed,

> The fact that the independent and dependent claims are in different statutory classes does not, in itself, render the latter improper. . . . Similarly, if claim 1 recites a method of making a product, a claim for a product made by the method of claim 1 could be a proper dependent claim.

As the foregoing sections of the Manual of Patent Examining Procedure indicate, dependent product-by-process claims are acceptable under 35 USC 112. Since Claims 26 and 27 are dependent product-by-process claims, the 35 USC 112 rejection of Claims 26 and 27 should be withdrawn.

Claims 1 - 5, 9, 12, and 26 have been rejected under 35 USC 102(b) as anticipated by Fiordalice et al. ("Fiordalice"), U.S. Patent 5,420,072. This rejection is respectfully traversed.

Independent Claim 1 recites a fabrication method in which a titanium nitride layer is formed over a substrate by physical vapor deposition to a thickness of less than 30 nm.

Referring parenthetically to col. 2, lines 21 - 47 and 61 - 63, of Fiordalice, the Examiner alleges that Fiordalice discloses a fabrication method in which a titanium nitride layer 22/24 is formed over a substrate by "physical vapor deposition" to a thickness of less than 30 nm. This is incorrect.

In the portion of the Detailed Description of a Preferred Embodiment at col. 2, line 21, through col. 4, line 17, Fiordalice discloses that titanium nitride layer 22 is formed on a

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substrate to a thickness of 5 - 100 nm and that titanium nitride layer 24 is formed on titanium nitride layer 22 likewise to a thickness of 5 - 100 nm. The composite thickness for titanium nitride layers 22 and 24 would thus appear to be 10 - 200 nm. However, Fiordalice discloses that layers 22 and 24 are formed by chemical vapor deposition ("CVD"), not physical vapor deposition ("PVD").

More particularly, Fiordalice states at col. 2, lines 56 - 61, that titanium nitride layer 22 is chemically vapor deposited. Slightly later at col. 2, lines 63 - 66, Fiordalice specifies that the deposition ambient, i.e., the vapor which acts as a source for the material deposited during Fiordalice's CVD, includes titanium tetrachloride, ammonia, nitrogen (diatomic), and argon.

Fiordalice does not appear to expressly state that titanium nitride layer 24 is chemical vapor deposited. However, Fiordalice states at col. 3, lines 43 - 51, that titanium nitride layer 24 is deposited *in situ* with titanium nitride layer 22 using a deposition ambient that includes titanium tetrachloride, ammonia, nitrogen, and argon. Since the deposition ambient utilized to form layer 24 is that same at that used to chemically vapor deposit layer 22, layer 24 is also formed by CVD. Hence, both of titanium nitride layers 22 and 24 are formed by CVD.

CVD is a deposition process in which a vapor formed with one or more chemical species that contain the material to be deposited, or components of the material to be deposited, undergoes suitable chemical reaction that enables the material being deposited to be released from the starting chemical species and accumulate on the deposition surface. In the preferred embodiment of Fiordalice, titanium nitride layers 22 and 24 are formed by chemical reaction in which the titanium tetrachloride undergoes chemical reaction to release titanium atoms which react chemically with nitrogen atoms provided from the ammonia and possibly the (diatomic) nitrogen.

PVD is a general term for a deposition process in which the material to be deposited is released from the source of the material largely by one or more physical mechanisms. Examples of PVD include sputtering, evaporation, pulsed laser deposition, and spraying.

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In any event, CVD is not PVD or a type of PVD. Since Fiordalice discloses that titanium nitride layers 22 and 24 are formed by CVD, the material which extends from col. 2, line 21, through col. 4, line 17, of Fiordalice, and which includes the portion of Fiordalice

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cited by the Examiner in regard to deposition of the titanium nitride layer, does not disclose the limitation of Claim 1 that the titanium nitride layer be formed by PVD to a thickness of less than 30 nm.

In the first paragraph of Fiordalice's background-art section, at col. 1, lines 11 - 27, Fiordalice mentions that layers of titanium nitride have been formed by sputter deposition. Although sputter deposition is a type of PVD, Fiordalice does not indicate that any such sputter deposited titanium nitride layer is less than 30 nm thick. Consequently, the background-art material disclosed at col. 1, lines 11 - 27, of Fiordalice does not meet the limitation of Claim 1 that the titanium nitride layer be formed by PVD to a thickness of less than 30 nm. Also, the background-art material of Fiordalice fails to disclose the further limitation of Claim 1 that a layer of tungsten be formed over the titanium nitride layer.

As far as Applicant's attorney can determine, nowhere does Fiordalice disclose a fabrication process in which a layer of titanium nitride is deposited by PVD to a thickness of less than 30 nm, let alone in conjunction with forming a tungsten layer over the titanium nitride layer. Accordingly, Fiordalice does not anticipate Claim 1.

Also, Fiordalice identifies various difficulties with sputter deposited titanium nitride layers created according to techniques that are prior art to Fiordalice. At col. 1, lines 19 - 27, Fiordalice states that:

> Sputter deposited titanium nitride, however, is not very conformal and its step coverage within high aspect ratio contacts and vias is poor, and as a result unacceptably thin or discontinuous titanium nitride barrier layers are formed within contacts and vias having high aspect ratios. Consequently, the reliability of high density integrated circuits fabricated with sputter deposited titanium nitride barrier layers and high aspect ratio contacts and vias is also poor.

Since sputtering is a type of PVD, Fiordalice teaches away from the PVD titanium nitride formation step of Claim 1. Consequently, Claim 1 is patentable over Fiordalice.

Claims 2 - 5, 9, and 12 all depend (directly or indirectly) from Claim 1. Hence, dependent Claims 2 - 5, 9, and 12 are patentable over Fiordalice for the same reasons as Claim 1.

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As to Claim 26, a titanium nitride layer created in the course of fabricating a structure according to the invention's teachings has advantageous characteristics, especially a reduced occurrence of volcanoes. See page 5 of the specification. When sputtering is the PVD technique employed to form the titanium nitride layer of the invention, the present titanium nitride layer also has a substantially columnar grain structure. As far as Applicant's attorney can determine, nothing in Fiordalice discloses that a titanium nitride layer deposited according to Fiordalice's CVD technique has the characteristics of the titanium nitride layer formed according to the invention's teachings. Consequently, Fiordalice does not anticipate Claim 26.

Additionally, nothing in Fiordalice would lead a person skilled in the art from a titanium nitride layer of the CVD-formed titanium nitride layers of Fiordalice to a titanium nitride layer having the characteristics that result when it is formed in accordance with the present invention. For example, nothing in Fiordalice indicates that any of Fiordalice's CVD titanium nitride layers has a columnar grain structure as occurs with the present sputter deposited titanium nitride layer. Consequently, Claim 26 is patentable over Fiordalice.

Claims 10 and 11 have been rejected under 35 USC 103 as obvious based on Fiordalice. This rejection is respectfully traversed.

Claims 10 and 11 both depend from Claim 1. As indicated above, nothing in Fiordalice discloses or suggests the limitation of Claim 1 that a titanium nitride layer be formed by PVD to a thickness of less than 30 nm. Accordingly, Claims 10 and 11 are patentable over Fiordalice for the same reasons that Claim 1 is patentable over Fiordalice.

Claims 6 - 8 have been rejected under 35 USC 103(a) as obvious based on Fiordalice in view of Yamamori, U.S. Patent 5,731,225. Claims 13, 21, 22, and 27 have been rejected under 35 USC 103(a) as obvious based on Fiordalice in view of Nagamine et al. ("Nagamine"), U.S. Patent 6,287,988. These rejections are respectfully traversed.

Claims 6 - 8, 13, 21, 22, and 27 all depend (directly or indirectly) from Claim 1. Again, repeating what was said above, nothing in Fiordalice discloses or suggests the limitation of Claim 1 that a titanium nitride layer be formed by PVD to a thickness of less than 30 nm.

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Yamamori discloses sputtering a layer of titanium nitride to a thickness of 50 - 200 nm. See col. 3, lines 29 - 32, of Yamamori. As far as Applicant's attorney can determine, Yamamori does not disclose the use of any PVD technique, such as sputtering, to form a titanium nitride layer having a thickness of less than 30 nm.

Nagamine does not appear to deal with the formation of titanium nitride layers. Hence, neither Yamamori nor Nagamine discloses the limitation of Claim 1 that a titanium nitride layer be formed by PVD to a thickness of less than 30 nm. Even if it were reasonable to combine Fiordalice with Yamamori or Nagamine, the combination would not teach the full subject matter of Claim 1. Since Claims 6 - 8 all depend from Claim 1, dependent Claims 6 - 8 are patentable over Fiordalice and Yamamori for the same reasons that Claim 1 is patentable over Fiordalice. Similarly, because Claims 13, 21, 22, and 27 all depend from Claim 1, dependent Claims 13, 21, 22, and 27 are patentable over Fiordalice and Nagamine for the same reasons that Claim 1 is patentable over Fiordalice.

New Claims 35 - 37 respectively depend from Claims 21, 26, and 27. Inasmuch as Claims 21, 26, and 27 have been shown to be patentable, dependent Claims 35 - 37 are patentable.

Claims 14 - 20 and 23 - 25 have been indicated as being allowable if rewritten in independent form. Claims 14 - 20 depend from Claim 1 by way of Claim 13. Claims 23 - 25 depend from Claim 21. Since Claims 1, 13, and 21 have been shown to be patentable over the applied art, Claims 14 - 20 and 23 - 25 are allowable in their current form.

In summary, the 35 USC 112 rejection of Claims 26 and 27 has been shown to inappropriate. Claims 1 - 13, 21, 22, 26, and 27 have been shown to be patentable over the applied art. The same applies to new Claims 35 - 37. Claims 14 - 20 and 23 - 25 are allowable in their present form. Consequently, Claims 1 - 27 and 35 - 37 should be allowed so that the application may proceed to issue.

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Respectfully submitted,

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APPENDIX

CLAIMS 6, 9, 13, 15, 18, 24, AND 25, WITH ANNOTATIONS TO INDICATE REVISIONS, OF U.S. PATENT APPLICATION 09/881,607, ATTORNEY DOCKET NO. M-11469 US

6. (Amended) The method of Claim 1 further comprising forming a titanium layer before forming the titanium nitride layer, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

9. (Amended) The method of Claim 1 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of at least [above] 600°C.

13. (Amended) The method of Claim 12 further comprising:

forming a circuit element in or over the substrate;

forming an insulating layer over the substrate and the circuit element;

forming an opening in the insulating layer, the opening exposing the circuit element, the opening comprising a trench at least 2 μm long;

wherein the titanium nitride layer and the tungsten layer extend into [are present in] the opening, and the tungsten layer electrically contacts the circuit element through material of the titanium nitride layer in the opening.

15. (Amended) The method of Claim 14 further comprising depositing a titanium layer over the insulating layer before forming [depositing] the titanium nitride layer, wherein the tungsten layer [in the opening] electrically contacts the circuit element through material of the titanium and titanium nitride layers in the opening.

18. (Amended) The method of Claim 14 wherein the circuit element comprises [a] metal or semiconductor material.

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24. (Amended) The method of Claim 21 wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a [in an ambient] temperature of about 670°C for 20-40 seconds.

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25. (Amended) The method of Claim 21 wherein heating the titanium nitride layer comprises heating the titanium nitride layer at a [in an ambient] temperature of about 620°C for 20 - 40 seconds.

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If time for consideration is requested arrangements should be made for a second telephone call, preferably within three working days.

When claims are selected, a formal multiplicity rejection is made, including a complete record of the telephone interview, followed by an action on the selected claims.

When applicant refuses to comply with the telephone request, a formal multiplicity rejection is made. The applicant's reply to a formal multiplicity rejection of the examiner, to be complete, must either:

(A) Reduce the number of claims presented to those selected previously by telephone, or if no previous selection has been made to a number not exceeding the number specified by the examiner in the Office action, thus overcoming the rejection based upon the ground of multiplicity, or

(B) In the event of a traverse of said rejection applicant, besides specifically pointing out the supposed errors of the multiplicity rejection, is required to confirm the selection previously made by telephone, or if no previous selection has been made, select certain claims for purpose of examination, the number of which is not greater than the number specified by the examiner.

If the rejection on multiplicity is adhered to, all claims retained will be included in such rejection and the selected claims only will be additionally examined on their merits. This procedure preserves applicant's right to have the rejection on multiplicity reviewed by the Board of Patent Appeals and Interferences.

Also, it is possible to reject one claim on an allowed claim if they differ only by subject matter old in the art. This ground of rejection is set forth in *Ex parte Whitelaw*, 1915 C.D. 18, 219 O.G. 1237 (Comm'r Pat. 1914). The *Ex parte Whitelaw* doctrine is restricted to cases where the claims are unduly multiplied or are substantial duplicates. *Ex parte Kochan*, 131 USPQ 204, 206 (Bd. App. 1961).

2173.05(o) Double Inclusion

There is no *per se* rule that "double inclusion" is improper in a claim. *In re Kelly*, 305 F.2d 909, 916, 134 USPQ 397, 402 (CCPA 1962) ("Automatic reliance upon a ' rule against double inclusion' will lead to as many unreasonable interpretations as will automatic reliance upon a 'rule allowing double inclusion' . The governing consideration is not *double inclusion*, but rather is what is a reasonable construction of the language of the claims."). Older cases, such as *Ex parte White*, 759 O.G. 783 (Bd. App. 1958) and *Ex parte Clark*, 174 USPQ 40 (Bd. App. 1971) should be applied with care, according to the facts of each case.

The facts in each case must be evaluated to determine whether or not the multiple inclusion of one or more elements in a claim gives rise to indefiniteness in that claim. The mere fact that a compound may be embraced by more than one member of a Markush group recited in the claim does not lead to any uncertainty as to the scope of that claim for either examination or infringement purposes. On the other hand, where a claim directed to a device can be read to include the same element twice, the claim may be indefinite. *Ex parte Kristensen*, 10 USPQ2d 1701 (Bd. Pat. App. & Inter. 1989).

2173.05(p) Claim Directed to Product-By-Process or Product and Process

There are many situations where claims are permissively drafted to include a reference to more than one statutory class of invention.

I. PRODUCT-BY-PROCESS

A product-by-process claim, which is a product claim that defines the claimed product in terms of the process by which it is made, is proper. *In re Luck*, 476 F.2d 650, 177 USPQ 523 (CCPA 1973); *In re Pilkington*, 411 F.2d 1345, 162 USPQ 145 (CCPA 1969); *In re Steppan*, 394 F.2d 1013, 156 USPQ 143 (CCPA 1967). A claim to a device, apparatus, manufacture, or composition of matter may contain a reference to the process in which it is intended to be used without being objectionable under 35 U.S.C. 112, second paragraph, so long as it is clear that the claim is directed to the product and not the process.

An applicant may present claims of varying scope even if it is necessary to describe the claimed product in product-by-process terms. *Ex parte Pantzer*, 176 USPQ 141 (Bd. App. 1972).

III. INFRINGEMENT TEST

The test as to whether a claim is a proper dependent claim is that it shall include every limitation of the claim from which it depends (35 U.S.C. 112, fourth paragraph) or in other words that it shall not conceivably be infringed by anything which would not also infringe the basic claim.

A dependent claim does not lack compliance with 35 U.S.C. 112, fourth paragraph, simply because there is a question as to (1) the significance of the further limitation added by the dependent claim, or (2) whether the further limitation in fact changes the scope of the dependent claim from that of the claim from which it depends. The test for a proper dependent claim under the fourth paragraph of 35 U.S.C. 112 is whether the dependent claim includes every limitation of the claim from which it depends. The test is not one of whether the claims differ in scope.

Thus, for example, if claim 1 recites the combination of elements A, B, C, and D, a claim reciting the structure of claim 1 in which D was omitted or replaced by E would not be a proper dependent claim, even though it placed further limitations on the remaining elements or added still other elements.

Examiners are reminded that a dependent claim is directed to a combination including everything recited in the base claim and what is recited in the dependent claim. It is this combination that must be compared with the prior art, exactly as if it were presented as one independent claim.

The fact that a dependent claim which is otherwise proper might relate to a separate invention which would require a separate search or be separately classified from the claim on which it depends would not render it an improper dependent claim, although it might result in a requirement for restriction.

The fact that the independent and dependent claims are in different statutory classes does not, in itself, render the latter improper. Thus, if claim 1 recites a specific product, a claim for the method of making the product of claim 1 in a particular manner would be a proper dependent claim since it could not be infringed without infringing claim 1. Similarly, if claim 1 recites a method of making a product, a claim for a product made by the method of claim 1 could be a proper dependent claim. On the other hand, if claim 1 recites a method of making a specified product, a claim to the product set forth in claim 1 would not be a proper dependent claim if the product might be made in other ways.

IV. CLAIM FORM AND ARRANGEMENT

A singular dependent claim 2 could read as follows:

2.The product of claim 1 in which . . . .

A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a *dependent* claim should not be separated therefrom by any claim which does not also depend from said "dependent claim." It should be kept in mind that a dependent claim may refer back to any preceding independent claim. These are are the only restrictions with respect to the sequence of claims and, in general, applicant's sequence should not be changed. See MPEP § 608.01(j). Applicant may be so advised by using form paragraph 6.18.

¶ 6.18 Series of Singular Dependent Claims

A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim which depends from a dependent claim should not be separated by any claim which does not also depend from said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

During prosecution, the order of claims may change and be in conflict with the requirement that dependent claims refer to a preceding claim. Accordingly, the numbering of dependent claims and the numbers of preceding claims referred to in dependent claims should be carefully checked when claims are renumbered upon allowance.

V. REJECTION AND OBJECTION

If the base claim has been canceled, a claim which is directly or indirectly dependent thereon should be rejected as incomplete. If the base claim is rejected, the dependent claim should be objected to rather than rejected, if it is otherwise allowable.

Form paragraph 7.43 can be used to state the objection.

PAGES 2 - 5, and 7

WITH ANNOTATIONS

TO INDICATE REVISIONS, OF U.S. PATENT APPLICATION 09/881,607

ATTORNEY DOCKET NO. M-11469 US

grains 150G in titanium nitride layer 150. During deposition of tungsten 160, the WF_6 molecules can diffuse between the TiN grains and react with titanium 140. This reaction produces titanium fluoride TiF_3. TiF_3 expands and causes failure of the TiN layer. The cracked TiN leads to a higher exposure of TiF_3 to WF_6, which in turn leads to the formation of volatile TiF_4. TiF_4 causes voids in the W film which are known as "volcanoes". To avoid the volcanoes, the sputtered titanium nitride layers have been made as thick as 40 nm, and at any rate no thinner than 30 nm. In addition, the sputtered titanium nitride layers have been annealed in nitrogen atmosphere to increase the size of the TiN grains.

SUMMARY

The inventor has ~~discovered~~ determined that under some conditions thinner annealed layers of sputtered titanium nitride unexpectedly provide better protection against the volcanoes than thicker layers. In some embodiments, fewer volcanoes have been observed with a TiN layer thickness of 20 nm than with 30 nm. In fact, no volcanoes have been observed in some structures formed with the 20 nm TiN layers. Why the thinner TiN layers provide better protection is not clear. Without limiting the invention to any particular theory, it is suggested that perhaps one reason is a lower stress in the thinner annealed layers and a higher density of the TiN grains.

The invention is applicable to physical vapor deposition techniques other than sputtering. Additional features and embodiments of the invention are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-3 are cross sectional views of prior art semiconductor structures in the process of fabrication.

Figs. 4-6 are cross sectional and perspective views of semiconductor structures in the process of fabrication according to one embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Fig. 4 is a cross sectional and perspective view of a dual damascene semiconductor structure in the process of fabrication according to one embodiment of the present invention. Layer 120 is polysilicon formed by chemical vapor deposition (CVD) over a monocrystalline silicon wafer 410. Before fabrication of layer 120, the

wafer 410 may have been processed to form devices such as MOS transistor 420. The transistor's source/drain regions 430 were formed in substrate 410, gate insulation 440 was formed over the substrate, and gate 450 was formed over the gate insulation. Other devices, including non-MOS devices, could be formed using known techniques. Layer 120 can also be part of substrate 410 (this embodiment is not shown in Fig. 4).

In the embodiment of Fig. 4, dielectric 460 was deposited over the wafer. Then layer 120 was formed as described above, and was patterned by a plasma etch. An exemplary thickness of layer 120 is 150 nm.

Dielectric layer 110 was deposited over the layer 120. In some embodiments, dielectric 110 was a combination of two silicon dioxide layers. The first layer was PSG (phosphosilicate glass) deposited by chemical vapor deposition (CVD). The second layer was silicon dioxide deposited by CVD from TEOS. The combined thickness of the two layers was approximately 900 nm.

Then a photoresist layer (not shown) was deposited and patterned photolithographically to define a via 464. In some embodiments, the mask opening defining the via was round in top view, with a diameter of 0.18 μm. The via was formed in layer 110 with a plasma etch.

The photoresist was removed, and another layer of photoresist (not shown) was deposited and patterned photolithographically to define a trench 470 in dielectric 110 for a tungsten interconnect. In some embodiments, the trench length was approximately 1 mm. The trench width was 0.22 μm. The trench was etched with a timed etch to a depth of approximately 250 nm. Via 464 was fully exposed at the bottom of the trench.

Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. The argon flow was 5 sccm (standard cubic centimeters per minute). The RF power was 313 W. This operation removed native oxide from layer 120. Also, this operation smoothened (rounded) top edges 480 of trench 470 and via 464. The rounded edges are desirable to reduce stress in titanium nitride 150 (Fig. 5) at these edges so as to reduce the risk of volcano formation. The RF plasma operation was performed in a system of type ENDURA available from Applied Materials of Santa Clara, California.

Then titanium layer 140 (Fig. 5) was sputter deposited from a titanium target. The sputtering was performed at a temperature of 200°C in argon atmosphere. The

base pressure (the pressure before the argon flow was turned on) was 5×10^{-7} torr. The DC power was 4000W, the RF power was 2500W. The wafer AC bias was 150W. The titanium deposition was performed in a system of type ENDURA, in an ionized metal plasma (IMP) chamber of type Vectra, available from Applied Materials.

The thickness of Ti layer 140 was varied. In one embodiment, the thickness was 10 nm. In another embodiment, the thickness was 36 nm. less than 36 nm, preferably less than 15 nm, more preferably less than 12 nm, typically

Then titanium nitride 150 was deposited by reactive sputtering from a titanium target in a nitrogen atmosphere. The base pressure (the pressure before the nitrogen flow was turned on) was 5×10^{-7} torr. The nitrogen flow was 28 sccm (standard cubic centimeters per minute), the DC power was 4000W, the RF power was 2500W, the wafer bias was 150W. The deposition temperature was 200°C. The deposition was performed in a system of type ENDURA, in an IMP chamber of type Vectra, available from Applied Materials.

The thickness of the TiN layer 150 was ~~20 nm in one embodiment,~~ 30 nm in another embodiment.

In one embodiment, the thickness of TiN layer 150 was less than 30 nm, preferably less than 25 nm, more preferably less than 22 nm, typically 20 nm.

Then the structure was heated to a temperature between 600°C and 700°C for 20 to 30 seconds, typically 20 to 40 seconds, in a nitrogen atmosphere. (This operation is referred to herein as Rapid Thermal Anneal, or RTA.) The base pressure was 100-120 torr, the nitrogen flow was 8 slm (standard liters per minute). The temperature was 620°C in one embodiment, 670°C in another embodiment. The anneal was performed in a system of type HEATPULSE 8800 available from AG Associates, Inc., of San Jose, California. The anneal is believed to have increased the lateral size of TiN grains 150G (Fig. 3).

Then tungsten layer 160 was deposited by CVD in two stages. At the first stage, the chemical reaction was:

$$2WF_6 + 3SiH_4 \rightarrow 2W + 3SiF_4 + 6H_2$$

This stage lasted 10 seconds. Then the silane (SiH_4) flow was turned off, and the hydrogen flow was turned on for the second stage. The chemical reaction was:

WF_6 (vapor) + $3H_2$ (vapor) → W (solid) + 6HF (vapor).

See S. Wolf, "Silicon Processing for the VLSI Era", vol. 2 (1990), page 246, incorporated herein by reference. Both stages were performed in a system of type CONCEPT 1 available from Novellus Systems of San Jose, California. The silane

flow was 20 sccm. The hydrogen flow was 12 - 15 slm (standard liters per minute). The WF_6 flow was 350 sccm. The pressure was 40 torr. The temperature was 400°C.

Then the layers 160, 150, 140 were polished off the top of dielectric ~~110~~ 110 by CMP. The resulting structure is shown in Fig. 6. Prior to CMP, the structure was examined for volcanoes using an optical microscope and SEM and STEM microscopes. The results are given in Table 1 below. The second column of Table 1 indicates the temperature of the Rapid Thermal Anneal, described above, performed after the deposition of TiN 150 before the deposition of tungsten 160. In Embodiment No. 1, the anneal was omitted.

Table 1

Embodiment No.	RTA of TiN	Ti/TiN thickness: 10 nm/20nm Volcanoes observed?	Ti/TiN thickness: 36 nm/30nm Volcanoes observed?
1.	None	Yes	Yes
2.	620°C	No	Yes, but fewer than in Embodiment No. 1
3.	670°C	No	No

These results show, unexpectedly, that the use of thinner Ti and TiN layers in combination with the RTA can provide a better protection against the volcanoes than thicker layers without the RTA. The thinner layers can eliminate the volcanoes at the lower RTA temperature of 620°C. Lower RTA temperatures are desirable to reduce impurity diffusion during the RTA, to prevent melting or softening of materials having low melting temperatures (e.g. aluminum), and reduce wafer warping.

In any event, the sputter deposited TiN layers, such as TiN layer 150, have substantially a columnar grain structure.

The invention is not limited to the particular materials, dimensions, structures, or fabrication processes described above. The invention is not limited to a thickness or composition of any particular layer, or the number, shape and size of vias 464 or trenches 470. The trench length, for example, is 2 μm in some embodiments, and other lengths are possible. The invention is not limited to the particular gas flow rates, temperatures, or any other fabrication parameters or equipment. Some embodiments use nitrogen sources other than pure nitrogen for the RTA or titanium nitride deposition. For example, ammonia (NH_3) or H_2/N_2 can be used. The invention is not limited to the Rapid Thermal Anneal or to any particular anneal

753474 v3
M-11469 US

I CLAIM:
~~CLAIMS~~

1. A fabrication method comprising:

forming a titanium nitride layer over a substrate by physical vapor deposition, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition.

2. The method of Claim 1 wherein the titanium nitride layer is formed by sputtering.

3. The method of Claim 2 wherein the titanium nitride layer is less than 25 nm thick.

4. The method of Claim 2 wherein the titanium nitride layer is less than 22 nm thick.

5. The method of Claim 2 wherein the titanium nitride layer is about 20 nm thick.

6. The method of Claim 1 further comprising forming a titanium layer before the titanium nitride layer, the titanium nitride layer being in physical contact with the titanium layer.

7. The method of Claim 6 wherein the titanium layer is less than 36 nm thick.

8. The method of Claim 6 wherein the titanium layer is about 10 nm thick.

9. The method of Claim 1 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature above 600°C.

10. The method of Claim 1 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 670°C for 20-40 seconds.

11. The method of Claim 1 wherein heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at a temperature of about 620°C for 20 - 40 seconds.

07-19-02

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Docket No.: M-11469 US

July 17, 2002

Commissioner For Patents
Washington, D.C. 20231

Re:	Applicant:	Fortin, Vincent		
	Assignee:	Mosel Vietlic, Inc.		
	Title:	Thin Titanium Nitride Layers Used in Conjunction With Tungsten		
	Serial No.:	09/881,607		
	Examiner:	Tran, Long K.	Filed:	June 13, 2001
	Docket No.:	M-11469 US	Group Art Unit:	2818

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

(1) Return Receipt Postcard;
(2) This Transmittal Letter (in duplicate);
(3) Response to Office Action (13 pgs.);
(4) Appendix (2 pgs.);
(5) Manual of Patent Examining Procedure, pg. 2100-205 (1pg.);
(6) Manual of Patent Examining Procedure, pg. 600-77 (1 pg.); and
(7) Specification pages 2 - 5, and page 7, with changes indicated in red.

☒ No additional fee is required.

CLAIMS AS AMENDED

Claims Remaining *After* Amendment		Highest No. Previously Paid For		Present Extra		Rate		Additional Fee
Total Claims	30	Minus	34	=	0	x	$18.00	$ 0.00
Independent Claims	2	Minus	3	=	0	x	$84.00	$ 0.00
☐ Fee of _____ for the first filing of one or more multiple dependent claims per application								$
☐ Fee for Request for Extension of Time								$
Total additional fee for this Amendment:								$ 0.00

☒ Conditional Petition for Extension of Time: If an extension of time is required for timely filing of the enclosed document(s) after all papers filed with this transmittal have been considered, an extension of time is hereby requested.

☒ Please charge our Deposit Account No. 19-2386 in the amount of $ 0.00

☒ Also, charge any additional fees required and credit any overpayment to our Deposit Account No. 19-2386.

Total: $ 0.00

EXPRESS MAIL LABEL NO.

EL 901 565 476 US

Respectfully submitted,

Ronald J. Meetin

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Attorney for Applicant
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879876 v1

A

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

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Washington, D.C. 20231

CHANGE OF ADDRESS/POWER OF ATTORNEY

8/ Change of Address
G. Stang
8-20-02

FILE LOCATION 28C1 SERIAL NUMBER 09881607 PATENT NUMBER

THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 24251

THE PRACTITIONERS OF RECORD HAVE BEEN CHANGED TO CUSTOMER # 24251

ON 07/05/02 THE ADDRESS OF RECORD FOR CUSTOMER NUMBER 24251 IS:

SKJERVEN MORRILL MACPHERSON LLP
25 METRO DRIVE
SUITE 700
SAN JOSE CA 95110

AND THE PRACTITIONERS OF RECORD FOR CUSTOMER NUMBER 24251 ARE:

24423	24486	25875	29089	29545	32892	33003	33938	34250	34691
34763	36320	37119	38321	39880	40218	40350	40494	40684	41008
41711	42117	42268	42381	42406	42622	43339	43817	44040	44047
44702	44881	44940	45591	45754	45906	45983	46030	46091	46341
46930	47026	47063	47548	48049	48375	48562			

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JUL 26 2002
TECHNOLOGY CENTER 2800

PTO INSTRUCTIONS: PLEASE TAKE THE FOLLOWING ACTION WHEN THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER NUMBER: RECORD, ON THE NEXT AVAILABLE CONTENTS LINE OF THE FILE JACKET, 'ADDRESS CHANGE TO CUSTOMER NUMBER'. LINE THROUGH THE OLD ADDRESS ON THE FILE JACKET LABEL AND ENTER ONLY THE 'CUSTOMER NUMBER' AS THE NEW ADDRESS. FILE THIS LETTER IN THE FILE JACKET. WHEN ABOVE CHANGES ARE ONLY TO FEE ADDRESS AND/OR PRACTITIONERS OF RECORD, FILE LETTER IN THE FILE JACKET.
THIS FILE IS ASSIGNED TO GAU 2818.

PTO-FMD
TALBOT-1/97

EXHIBIT I

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Washington, D.C. 20231
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/881,607	06/13/2001	Vincent Fortin	M-11469 US	6406

24251 7590 12/27/2002

SKJERVEN MORRILL LLP
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EXAMINER
TRAN, LONG K

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

Office Action Summary	Application No. 09/881,607	Applicant(s) FORTIN, VINCENT
	Examiner Long K. Tran	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b)

Status

1)☒ Responsive to communication(s) filed on *26 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-27 and 35-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-27 and 35-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a)☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4)☐ Interview Summary (PTO-413) Paper No(s). _____ .
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

Response to Amendment

1. This office action is in response to Amendment filed on October 26, 2002.

2. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

3. Claims **28 – 34** have been cancelled in Paper No. **7**.

4. Claims **35 – 37** have been added in Paper No. **7**.

5. Claims **6, 9, 13, 15, 18, 24** and **25** have been amended in Paper No. **7.**

6. Claim **3** has been cancelled in Paper No. **11**.

7. Claims **1, 6, 12, 13, 14, 15** and **20** have been amended in Paper No. **11.**

8. Claims **38 – 52** have been added in Paper No. **11**

9. Claims **1, 2, 4 – 27** and **35 – 52** are presented for examination.

Information Disclosure Statement

10. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on November 26, 2002

Information disclosed and lists on PTO 1449 were considered.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims **1, 2, 4 – 18, 21 – 27, 35, 38 – 48** and **51** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. (US Patent No. 6,110,789) in view of Chen (US Patent No. 6,136,691).

Regarding claims **1, 2, 4, 5, 6, 7, 8, 21, 38, 39, 40** and **41**, Rhode et al. disclose a fabrication method comprising: forming a circuit element in or over a semiconductor substrate; forming an insulating layer over the circuit element, forming an opening in the insulating layer to expose the circuit element at the bottom of the opening; forming a 50 Å to 300 Å thick titanium layer over the insulating layer, the titanium layer overlaying sidewalls of opening; forming a 50 Å to 500 Å thick titanium nitride layer upper 350 (fig. 3C ; col. 5, lines 16- 44) over a structure by physical vapor deposition (sputtering; claim 13) such that the titanium nitride layer extends at least into an opening 340 (fig. 3C); heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound (col. 5, lines 45 - 64); forming a tungsten layer 355 (fig. 3D) over and in physical contact with the titanium nitride layer 350 (fig. 3D) such that the tungsten layer also extends at least into the opening in the structure (col. 6, lines 19-29).

Rhode et al. do not explicitly teach the use of CVD method for filling tungsten for forming plug. It is conventional and also taught by Chen that CVD or PVD is a method for depositing tungsten into plug (Chen: col. 1, lines 33-34).

Regarding claims **9 – 11, 24, 25, 35, 42,** and **43**, Rhode et al. disclose heating the titanium nitride layer comprises exposing the titanium nitride layer to the nitrogen and/or the nitrogen compound at temperature about 650° C to about 800° C with a

duration about 1 second to about 2 minutes and is advantageously about 20 seconds (col. 5; lines 46 – 64).

Regarding claims **26, 27** and **51,** the structure of claims 26, 27 and 51 are rejected as the same as the rejection of claims 1; 21 and 38 above.

Regarding claims **13, 12, 22, 23, 44** and **46**, Rhodes et al. and Chen disclose the claimed invention except for the trench is at least 2 μm long; at least 1mm long.

It would have been obvious to one of ordinary skill in the art to provide the trench having a length in the range as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPTO 233.

Regarding claims **12** and **45**, Rhode et al. disclose substrate is a semiconductor (col. 3, lines 39 –51).

Regarding claims **15, 16, 17, 18, 47** and **48**, Rhodes et al. disclose before forming the titanium nitride layer, depositing a titanium layer over the insulating layer such that the titanium layer extends at least into an opening in the insulating layer and such that the tungsten layer electrically contacts the circuit element through material of titanium and titanium nitride layers in the opening in the insulating layer; the trench does not penetrate the insulating layer but a via at the bottom of the trench penetrates the insulating and exposes the circuit element which is conductive comprising semiconductor material, wherein the titanium layer physically contacts the circuit element at the bottom of the via (figs. 2, 3E; col.1, lines 12 – 34 and col. 4, lines 31+).

13. Claims **19, 20, 36, 37, 49, 50** and **52** are rejected under 35 U.S.C. 103(a) as being unpatentable over Rhodes et al. (US Patent No. 6,110,789) in view of Chen (US Patent No. 6,136,691) and further in view of Yu (US patent No. 5,654,233).

Regarding claims **19, 20, 49** and 50, Rhode et al., Chen disclose the claimed invention except for rounding top edges of the trench and the via.

Yu discloses a step providing a dry etch process to remove partially the thick electrically conductive film around the top portion of the opening to allow more deposition of subsequent barrier layer or via hole metal in the lower portion of the hole (col.2, line 66+, col.3, lines1+). It is well settled that, the change in shape of the trench corner was a matter of design choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the paticular configuration of the trench was significant. *In re Dailey*, 357 F.2d 669, 149 USPTO 47 (CCPA 1996).

Regarding claims **36, 37** and **52**, Yu discloses the titanium nitride layer has a substantially columnar grain structure (col. 3, lines 44 –51).

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 703-305-5482. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 703-308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7466 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3329.

Long Tran LT

December 20, 2002

HOAI HO
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/881,607	Applicant(s)/Patent Under Reexamination FORTIN, VINCENT	
	Examiner Long K. Tran	Art Unit 2818	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,110,789	08-2000	Rhodes et al.	438/305
	B	US-6,136,691	10-2000	Chen, Chang-Hui	438/627
	C	US-5,552,339	09-1996	Hsieh, Shih-Huang	438/643
	D	US-6,319,826	11-2001	Chen et al.	438/653
	E	US-5,420,072	05-1995	Fiordalice et al.	438/607
	F	US-6,475,907	11-2002	Taguwa, Tetsuya	438/648
	G	US-5,654,233	08-1997	Yu, Chen-Hua Douglas	438/643
	H	US-4,960,732	10-1990	Dixit et al.	
	I	~~US-6,475,907~~	~~11-2002~~	~~Taguwa, Tetsuya~~	~~438/648~~
	J	US-6,146,991	11-2000	Cheng et al.	438/622
	K	US-6,333,261	12-2001	Lin et al.	438/656
	L	US-6,150,257	11-2000	Yin et al.	438/622
	M	US-5,731,225	03-1998	Yamamori, Atsushi	438/653

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707 05(a))
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EXHIBIT J

#15/Amdt C 4.30.03 CMoore

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Fortin, Vincent		
Assignee:	Mosel Vitelic, Inc.		
Title:	Thin Titanium Nitride Layers Used In Conjunction With Tungsten		
Serial No.:	09/881,607	Filing Date:	June 13, 2001
Examiner:	Tran, Long K.	Group Art Unit:	2818
Docket No.:	M-11469 US	Confirmation No.:	6406

Mountain View, California
27 March 2003

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

AMENDMENT

Responsive to the Office Action mailed 27 December 2002, please amend the above patent application as follows:

IN THE SPECIFICATION

Page 3, amend the paragraph beginning at line 24 to read

--Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. The argon flow was 5 sccm (standard cubic centimeters per minute). The RF power was 315 W. This operation removed native oxide from layer 120. Also, this operation smoothened (rounded) top edges 480 of trench 470 and via 464, i.e., the respective perimetrical top edges formed by the perimeters of trench 470 and via 464 along the surfaces into which they respectively extend. The rounded perimetrical top edges are desirable to reduce stress in titanium nitride 150 (Fig. 5) at these edges so as to reduce the risk of volcano formation. The RF plasma operation was performed in a system of type ENDURA available from Applied Materials of Santa Clara, California.--

Enclosed is a copy of specification page 3 in which the changes to the foregoing paragraph are indicated in red.

Ronald J. Meetin
Attorney at Law
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Mountain View, CA
94043-4869
Tel 650-964-9767
Fax 650-964-9779

IN THE CLAIMS

Amend Claim 1 to read:

--1. (Twice amended) A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 25 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.--

Cancel Claim 19 without prejudice.

Amend Claims 20, 21, and 38 to read:

-20. (Twice amended) The method of Claim 14 wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.

21. (Amended) A method for fabricating an integrated circuit, the method comprising:

forming a circuit element in or over a semiconductor substrate;

forming an insulating layer over the circuit element;

forming an opening through the insulating layer to expose the circuit element at the bottom of the opening, the opening having a perimetrical top edge that extends along an exterior surface of the insulating layer;

rounding the top edge of the opening;

forming a titanium layer over the insulating layer, the titanium layer overlaying side and bottom surfaces of the opening, the titanium layer being less than 15 nm thick;

forming a titanium nitride layer over the titanium layer, the titanium nitride layer being less than 25 nm thick, the titanium nitride layer being formed by sputtering;

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heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and

forming a tungsten layer by chemical vapor deposition over the titanium nitride layer, the tungsten layer at least partially filling the opening and electrically contacting the circuit element through the titanium and titanium nitride layers.

~~38~~. (Amended) A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer to a temperature above 600°C while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.--

Cancel Claim ~~49~~ without prejudice.

Amend Claim 50 to read:

--~~50~~. (Amended) The method of Claim ~~49~~ wherein the opening in the structure includes a via at the bottom of the trench, the method further comprising rounding the via along its perimetrical top edge.--

Enclosed is an appendix which indicates how the above version of Claims 1, 20, 21, 38, and 50 is produced from the previous version of those claims. In the appendix, added material is underlined, and deleted material is in brackets.

Add new Claims 53 - 64 as follows:

--~~53~~. The method of Claim 1 where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

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54. The method of Claim 53 wherein the tungsten halide comprises tungsten hexafluoride.

55. The method of Claim 38 where the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

56. The method of Claim 56 wherein the tungsten halide comprises tungsten hexafluoride.

57. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

58. The method of Claim 57 wherein the titanium nitride layer is formed by sputtering.

59. The method of Claim 57 further comprising, before forming the titanium nitride layer, forming a titanium layer over the structure such that the titanium layer extends at least into the opening in the structure, the titanium nitride layer being subsequently formed so as to be in physical contact with the titanium layer.

60. The method of Claim 57 wherein the chemical vapor deposition of the tungsten layer comprises reacting a tungsten halide with silane and subsequently with hydrogen.

61. The method of Claim 60 wherein the tungsten halide comprises tungsten hexafluoride.

62. A fabrication method comprising:

forming a titanium nitride layer over a structure by physical vapor deposition such that the titanium nitride layer extends at least into an opening in the structure, the titanium nitride layer being less than 30 nm thick;

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heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening, the chemical vapor deposition of the tungsten layer comprising reacting a tungsten halide with silane and subsequently with hydrogen.

~~63~~ 53. The method of Claim ~~62~~ 52 wherein the tungsten halide comprises tungsten hexafluoride.

~~64~~ 54. The method of Claim ~~62~~ 52 wherein the titanium nitride layer is formed by sputtering.--

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REMARKS

The specification has been revised to avoid singular-versus-plural difficulties with respect to what is meant by the "top edges" of trench 470 and via 464. In particular, an opening which extends from the top surface of a body partway into the body and which is shaped, for example, like a polygon as viewed perpendicular to the body' top surface can be considered as having only one top edge or (due to the polygonal shape) as having multiple top edges. This potential singular-versus-plural unclarity can be avoided by describing the top of the opening in terms of the "perimetrical top edge" formed by the perimeter of the opening along the body's top surface. Such terminology has been introduced into the specification with regard to trench 470 and via 464 in order to avoid unclarity as to the meaning of their "top edges" and to make it clear how "perimetrical top edge" language for openings recited in the present claims is supported in the specification.

Claims 1, 20, 21, 38, and 50 have been amended. Claims 19 and 49 have been canceled. Claims 53 - 64 have been added. Accordingly, Claims 1, 2, 4 - 18, 20 - 27, 35 - 48, and 50 - 64 are now pending.

Claims 1, 2, 4 - 18, 21 - 27, 35, 38 - 48, and 51 have been rejected under 35 USC 103(a) as obvious based on Rhodes et al. ("Rhodes"), U.S. Patent 6,110,789, in view of Chen, U.S. Patent 6,136,691. Claims 19, 20, 36, 37, 49, 50, and 52 have been rejected under 35 USC 103(a) as obvious based on Rhodes in view of Chen and Yu, U.S. Patent 5,654,233. These rejections are respectfully traversed in view of the revisions to the claims.

Rhodes discloses a contact-forming procedure in which contact hole 340 is formed through insulative layer 335 down to underlying semiconductor material. Barrier layer 350 is provided on insulative layer 335 and in contact hole 340 so as to coat its bottom and side surfaces. Barrier layer consists of (a) a lower titanium sublayer whose thickness varies from 5 - 30 nm at the bottom of hole 340 to 100 - 150 nm at the top of hole 340 and along the upper surface of insulative layer 335 and (b) an upper titanium nitride sublayer whose thickness varies from 5 - 20 nm at the bottom of hole 340 to 10 - 50 nm at the top of hole 340 and along the upper surface of the lower titanium sublayer. Rhodes specifies that the upper titanium nitride sublayer can be formed by any one of several techniques including physical vapor deposition ("PVD") in which titanium nitride is deposited by sputtering from a titanium

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nitride target or by (reactive) sputtering from a titanium target in a nitrogen-containing atmosphere.

Subsequent to forming the upper titanium nitride sublayer, Rhodes anneals the structure. The anneal is a rapid thermal anneal at 650 - 800°C, typically 725°C, for 1 - 120 sec., typically 20 sec., or a furnace anneal at 600 - 850°C for 1 - 60 min. In one embodiment, the anneal is performed in a nitrogen atmosphere. Rhodes indicates that the anneal can alternatively be performed in a mixture of nitrogen and hydrogen. Electrically conductive material, typically tungsten, is deposited on barrier layer 350 and into contact hole 340 to fill the remainder of hole 340. The material extending out of hole 340 is removed by a suitable technique such as chemical-mechanical polishing.

Chen discloses a contact-forming procedure in which contact hole 16 is formed in insulating layer 12. Titanium layer 18 is sputter deposited to a thickness of 10 - 80 nm. Titanium nitride layer 20 is formed by PVD or chemical vapor deposition ("CVD") to a thickness of 40 - 100 nm. Tungsten layer 22 is then formed by CVD in which tungsten hexafluoride is reacted with silane. The tungsten protruding out of contact hole 16 is removed.

Yu discloses a contact/via-forming procedure in which opening 11 (or 10) is formed through silicon oxide layer 12 and into silicon substrate 9. A cleaning step is performed to clean the upper surface of the structure without deteriorating the exposed silicon oxide or the silicon exposed through opening 11. Titanium layer 14 is formed. Titanium nitride layer is formed by CVD to a thickness of 30 - 140 nm.

A reactive-ion etch ("RIE") is performed to remove overhanging material of titanium nitride layer 15. After performing a cleaning step to remove RIE residue, titanium nitride layer 16 is formed by PVD to a thickness of 3 - 8 nm. Yu then deposits tungsten on titanium nitride layer 16 and into opening 11 to fill the remainder of opening 11.

Independent Claims 1 and 38, as amended, respectively recite:

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1. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the structure by physical vapor deposition such that the titanium nitride layer extends at least into the opening, the titanium nitride layer being less than 25 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening.

38. A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over a structure by physical vapor deposition such that the titanium nitride layer extends at least into an opening in the structure, the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer to a temperature above 600°C while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening in the structure.

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The new material in each of Claims 1 and 38 is the first two acts which specify (a) that the recited structure is provided with an opening extending partway through the structure and (b) that the top edge of the opening is rounded. The recitation that the opening has "a perimetrical top edge extending along an exterior surface of the structure" is a procedural

clause intended to make it clear that the recited "top edge" of the opening means the perimeter of the opening extending along the structure's exterior surface.

Claims 19 and 49, now cancelled, respectively depended from Claims 1 and 38. Dependent Claims 19 and 49 each recited the act of rounding the top edges of a trench for the situation in which the opening in the structure comprised the trench. Amended Claim 1 thus basically constitutes an independent version of Claim 19 subject to broadening the trench of Claim 19 to the opening of Claim 1 and subject to the clarifying language in the first act of Claim 1. Amended Claim 38 is similarly basically an independent version of Claim 49 subject to broadening the trench of Claim 49 to the opening of Claim 38 and subject to the clarifying language in the first act of Claim 38.

Cancelled Claims 19 and 49 were, as indicated above, rejected as obvious based on Rhodes, Chen, and Yu. With reference to Claims 19 and 49, the Examiner noted on page 5 of the Office Action that Rhodes and Chen do not disclose "rounding top edges of the trench and the via". The Examiner then stated that "Yu discloses a step providing a dry etch process to remove partially the thick electrically conductive film around the top portion of the opening to allow more deposition of substrate barrier layer or via hole metal in the lower portion of the hole (col. 2, line 66+, col. 3, lines 1+)" and that "It is well settled that, the change in shape of the trench corner was a matter of design choice which a person of ordinary skill in the art would have found obvious absent persuasive evidence that the paticular [sic] configuration of the trench was significant". Applicant's Attorney believes, however, that Claims 19 and 49 were patentable over Rhodes, Chen, and Yu and, accordingly, that amended Claims 1 and 38 are patentable over Rhodes and Chen separately or combined with Yu.

Firstly, the portion (col. 2, line 66+, through col. 3, line 1+) of Yu cited by the Examiner recites that "It is yet another object of this invention to provide a dry etch process to remove partially the thick electrically conductive film that protrudes and overhangs around the top edge of the via opening, and around the wall near the top of the small contact hole, but not reduce the thickness of the thin barrier layer at the bottom or around the lower portion of the wall of the small contact hole". This material is a summary version of the disclosure at col. 4, line 65, through col. 5, line 14, where Yu describes the RIE utilized to remove overhanging material of titanium nitride layer 15. The overhanging titanium nitride is

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illustrated in Fig. 2A (or 2B) of Yu. Fig. 3A (or 3B) of Yu illustrates how Yu's structure appears after the RIE is performed to remove the overhanging titanium nitride.

Rhodes does not disclose any overhanging portion of the titanium nitride sublayer of barrier layer 350. Chen likewise does not disclose any overhanging portion of titanium nitride layer 20. Hence, there would be no reason to apply the teachings of Yu to Rhodes and Chen in the manner proposed by the Examiner with respect to Claims 19 and 49. That is, it would not be obvious to combine Rhodes, Chen, and Yu in the indicated manner. This is one reason why Claims 19 and 49 would have been patentable over Rhodes, Chen, and Yu. Since Claims 1 and 38 basically respectively incorporate the rounding-act limitations of Claims 19 and 49, this is also one reason why Claims 1 and 38 are patentable over Rhodes and Chen separately or in combination with Yu.

Secondly, Claims 1 and 38 each recite that the top edge of the opening in the structure is rounded at a point prior to the deposition of the titanium nitride layer. In contrast, Yu deals with modifying the shape of titanium nitride layer 15. Yu does not disclose any rounding of the top edge of opening 11. Even if there were some reason for combining Rhodes, Chen, and Yu, the combination would not teach the full subject matter of Claim 1 or 38. This is another reason why Claims 1 and 38 are patentable over Rhodes and Chen separately or taken with Yu.

Thirdly, the present invention is directed toward reducing the incidence of voids, referred to as volcanoes, in the tungsten layer as provided on page 2 of the specification. Rounding the top edges of the contact/via openings helps decrease the likelihood of volcano formation. See the last full paragraph on page 3 of the specification where it is stated that:

> Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. . . . This operation removed native oxide from layer 120. Also, this operation smoothened (rounded) top edges 480 of trench 470 and via 464. The rounded edges are desirable to reduce stress in titanium nitride 150 (Fig. 5) at these edges so as to reduce the risk of volcano formation.

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The specification goes on to describe how titanium layer 140, titanium nitride layer 150, and tungsten layer 160 are formed after rounding the top edges of trench 470 and via 464. Since

trench 470 implements the opening in the structure recited in Claim 1 or 38, rounding the top edge of that opening helps achieve a major objective of the invention.

In short, the top-edge rounding act recited in Claim 1 or 38 is not merely an act performed as a matter of design choice. Instead, the rounding act is a significant factor in achieving the volcano-reduction objective of the invention. Nothing in Yu discloses or suggests that rounding the top edge of an opening that receives tungsten would help alleviate volcano formation. The absence of such a disclosure or suggestion combined with the significant nature of the rounding act in Claim 1 or 38 is further reason why Claims 1 and 38 are patentable over Rhodes and Chen separately or taken with Yu.

Independent Claim 21, which has been rejected on the basis of Rhodes and Chen, has been revised in a manner similar to that of Claims 1 and 38. Claim 21 now recites that the top edge of the opening in the insulating layer is rounded. The opening in the insulating layer in Claim 21 corresponds to the opening in the structure of Claim 1 or 38. Consequently, Claim 21 is patentable over Rhodes and Chen separately or in combination with Yu for the same reasons as Claims 1 and 38.

Claims 2, 4 - 18, 20, 22 - 27, 35 - 37, and 39 - 52 variously depend (directly or indirectly) from Claims 1, 21, and 38. Dependent Claims 2, 4 - 18, 20, 22 - 27, 35 - 37, and 39 - 52 are thus patentable over Rhodes and Chen separately or in combination with Yu for the same reasons as Claims 1, 21, and 38.

Dependent Claims 16, 20, 48, and 50 each recite a via at the bottom of a trench. As far as Applicant's Attorney can determine, none of Rhodes, Chen, and Yu discloses or suggests such a trench/via structure. Contrary to what is alleged in the last paragraph on page 4 of the Office Action, Rhodes does not appear to disclose or suggest such a structure in Fig. 2 or 3E or in the text at col. 1, lines 12 - 34, or col. 4, lines 31 - 36. The cited portions of Rhodes disclose a contact opening or a via, not the combination of a trench and a via physically distinguishable from the trench. Claims 16, 20, 48, and 50 are therefore separately patentable over Rhodes and Chen separately or combined with Yu.

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In addition to the above-mentioned revisions to the claims, several minor changes have been made to the claims to clarify their wording. This includes modifying dependent

Claims 19 and 49 to employ "perimetrical" top-edge language of the type used in independent Claims 1 and 38.

Turning to the new claims, independent Claim 57 repeats the first two acts, i.e., the opening-forming act and the top-edge rounding act, of each of Claims 1 and 38. As a consequence, Claim 57 is patentable over Rhodes and Chen separately or in combination with Yu for the same reason as Claims 1 and 38. The same applies to Claims 58 - 61 since they depend (directly or indirectly) from Claim 57.

New Claims 53 - 56 are dependent claims that variously depend (directly or indirectly) from Claims 1 and 38. Accordingly, dependent Claims 53 - 56 are patentable over Rhodes and Chen separately or taken with Yu for the same reasons as Claims 1 and 38.

Additionally, dependent Claims 53 - 56, 60, and 61 all require that the tungsten layer be formed by CVD in which a tungsten halide is initially reacted with silane and then with hydrogen. None of Rhodes, Chen, and Yu discloses or suggests this way of implementing tungsten CVD. This furnishes a separate basis for allowing Claims 53 - 56, 60, and 61 over Rhodes and Chen separately or in combination with Yu.

New Claims 62 - 64, including independent Claim 62, require that a tungsten layer provided over a PVD-formed titanium nitride layer whose thickness is no more than 30 nm be similarly formed by CVD in which a tungsten halide is initially reacted with silane and then with hydrogen. Inasmuch as this way of implementing tungsten CVD is not disclosed in any of Rhodes, Chen, and Yu, Claims 62 - 64 are patentable over the three references.

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In summary, all of pending Claims 1, 2, 4 - 18, 20 - 27, 35 - 48, and 50 - 64 have been shown to be patentable over the applied art. Claims 1, 2, 4 - 18, 20 - 27, 35 - 48, and 50 - 64 should therefore be allowed so that the case may proceed to issue.

Please telephone Applicant's Attorney at 650-964-9767 if there are any questions.

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APPENDIX

CLAIMS 1, 20, 21, 38, AND 50,
WITH ANNOTATIONS TO INDICATE REVISIONS, OF
U.S. PATENT APPLICATION 09/881,607,
ATTORNEY DOCKET NO. M-11469 US

1. (Twice amended) A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the [a] structure by physical vapor deposition such that the titanium nitride layer extends at least into the [an] opening [in the structure], the titanium nitride layer being less than 25 nm thick;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening [in the structure].

20. (Twice amended) The method of Claim 14 wherein the opening in the structure includes a via at the [a] bottom of the trench, the method further comprising rounding [top edges of the trench and] the via along its perimetrical top edge.

21. (Amended) A method for fabricating an integrated circuit, the method comprising:

forming a circuit element in or over a semiconductor substrate;

forming an insulating layer over the circuit element;

forming an opening through [in] the insulating layer to expose the circuit element at the [a] bottom of the opening, the opening having a perimetrical top edge that extends along an exterior surface of the insulating layer;

rounding the top edge of the opening;

forming a titanium layer over the insulating layer, the titanium layer overlaying side and bottom surfaces [sidewalls] of the opening, the titanium layer being less than 15 nm thick;

forming a titanium nitride layer over the titanium layer, the titanium nitride layer being less than 25 nm thick, the titanium nitride layer being formed by sputtering;

heating the titanium nitride layer while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and

forming a tungsten layer by chemical vapor deposition over the titanium nitride layer, the tungsten layer at least partially filling the opening and electrically contacting the circuit element through the titanium and titanium nitride layers.

38. (Amended) A fabrication method comprising:

providing a structure with an opening that extends partway through the structure, the opening having a perimetrical top edge that extends along an exterior surface of the structure;

rounding the top edge of the opening;

forming a titanium nitride layer over the [a] structure by physical vapor deposition such that the titanium nitride layer extends at least into the [an] opening [in the structure], the titanium nitride layer being less than 30 nm thick;

heating the titanium nitride layer to a temperature above 600°C while exposing the titanium nitride layer to nitrogen and/or a nitrogen compound; and then

forming a tungsten layer over and in physical contact with the titanium nitride layer by chemical vapor deposition such that the tungsten layer also extends at least into the opening [in the structure].

50. (Amended) The method of Claim 46 wherein the opening in the structure includes a via at the [a] bottom of the trench, the method further comprising rounding [top edges of the trench and] the via along its perimetrical top edge.

PAGE 3,

WITH ANNOTATIONS

TO INDICATE REVISIONS,

OF U.S. PATENT APPLICATION 09/881,607

ATTORNEY DOCKET NO. M-11469 US

wafer 410 may have been processed to form devices such as MOS transistor 420. The transistor's source/drain regions 430 were formed in substrate 410, gate insulation 440 was formed over the substrate, and gate 450 was formed over the gate insulation. Other devices, including non-MOS devices, could be formed using known techniques. Layer 120 can also be part of substrate 410 (this embodiment is not shown in Fig. 4).

In the embodiment of Fig. 4, dielectric 460 was deposited over the wafer. Then layer 120 was formed as described above, and was patterned by a plasma etch. An exemplary thickness of layer 120 is 150 nm.

Dielectric layer 110 was deposited over the layer 120. In some embodiments, dielectric 110 was a combination of two silicon dioxide layers. The first layer was PSG (phosphosilicate glass) deposited by chemical vapor deposition (CVD). The second layer was silicon dioxide deposited by CVD from TEOS. The combined thickness of the two layers was approximately 900 nm.

Then a photoresist layer (not shown) was deposited and patterned photolithographically to define a via 464. In some embodiments, the mask opening defining the via was round in top view, with a diameter of 0.18 μm. The via was formed in layer 110 with a plasma etch.

The photoresist was removed, and another layer of photoresist (not shown) was deposited and patterned photolithographically to define a trench 470 in dielectric 110 for a tungsten interconnect. In some embodiments, the trench length was approximately 1 mm. The trench width was 0.22 μm. The trench was etched with a timed etch to a depth of approximately 250 nm. Via 464 was fully exposed at the bottom of the trench.

Then the top surface of the structure was exposed to RF plasma in argon atmosphere for 10 seconds. The argon flow was 5 sccm (standard cubic centimeters per minute). The RF power was 315 W. This operation removed native oxide from layer 120. Also, this operation smoothened (rounded) top edges 480 of trench 470 and via 464. The rounded edges are desirable to reduce stress in titanium nitride 150 (Fig. 5) at these edges so as to reduce the risk of volcano formation. The RF plasma operation was performed in a system of type ENDURA available from Applied Materials of Santa Clara, California.

Then titanium layer 140 (Fig. 5) was sputter deposited from a titanium target. The sputtering was performed at a temperature of 200°C in argon atmosphere. The

perimetrical top

, i.e., the respective perimetrical top edges formed by the perimeters of trench 470 and via 464 along the surfaces into which they respectively extend

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27 March 2003

Commissioner for Patents
Washington, D.C. 20231

Re:	Application No.:	09/881,607	Confirmation No.:	6406
	First Named Inventor:	Fortin, Vincent	Filing Date:	13 June 2001
	Group Art Unit:	2818	Examiner:	Tran, Long K.
	Atty. Docket No.:	M-11469 US		
	Title:	Thin Titanium Nitride Layers Used In Conjunction With Tungsten		
	Assignee(s):	Mosel Vitelic, Inc.		

Sir:

Transmitted herewith are the following documents for the above patent application:

(1) Return Receipt Postcard
(2) This Transmittal Letter (in duplicate)
(3) Amendment (13 pg(s).)
(4) Appendix (2 pg(s).)
(5) Annotated Specification Change Cover Sheet (1 pg.)
(6) Specification Page 3 with Changes Indicated in Red (1 pg.)

☒ The fee has been calculated as shown below:

CLAIMS AS AMENDED

	Claims Remaining *After* Amendment		Highest No. Previously Paid For		Present Extra		Rate		Additional Fee
Total Claims	54	Minus	44	=	10	×	18.00	$	180.00
Independent Claims	5	Minus	3	=	2	×	84.00	$	168.00
☐ Fee of $280 for the first filing of one or more multiple dependent claims								$	
☐ Fee for Request for Extension of Time (month(s))								$	
☐ Fee for								$	
Total additional fee for this Amendment:								$	348.00
☒ Please charge Deposit Account No. 502641 in the amount of								$	348.00

☐ Conditional Petition for Extension of Time: If an extension of time is required, the Commissioner is authorized to deduct the necessary fee from Deposit Account No. 502641.

☐ Also, charge any additional fees required and credit any overpayment to Deposit Account No. 502641.

☐ Enclosed is a check in the amount of $

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CERTIFICATE OF SERVICE

I hereby certify that on November 6, 2007, I caused the foregoing to be electronically filed with the Clerk of the Court using CM/ECF which will send electronic notification of such filing to the following:

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Additionally, I hereby certify that true and correct copies of the foregoing were caused to be served on November 6, 2007 upon the following individuals in the manner indicated:

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